# Design Example Report

<table>
<thead>
<tr>
<th>Title</th>
<th>15 W Isolated Flyback Power Supply with StackFET Using InnoSwitch™ 3-AQ INN3996CQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification</td>
<td>30 VDC – 1200 VDC Input; 12 V / 1.25 A Output (&gt;60 VDC Input)</td>
</tr>
<tr>
<td>Application</td>
<td>High Input Voltage for Automotive</td>
</tr>
<tr>
<td>Author</td>
<td>Applications Engineering Department</td>
</tr>
<tr>
<td>Document Number</td>
<td>DER-889Q</td>
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<tr>
<td>Date</td>
<td>August 10, 2021</td>
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<tr>
<td>Revision</td>
<td>1.3</td>
</tr>
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</table>

**Summary and Features**
- High input voltage: up to 1200 VDC
- InnoSwitch3-AQ – industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >82% efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing

PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations’ patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using a DC supply to provide the DC input to the prototype board.
1 Introduction
This document is an engineering report describing a 30 VDC to 1200 VDC input, 12 V output, 15 W (maximum) power supply utilizing INN3996CQ from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.

Figure 1 – Populated Circuit Board Photograph, Top.

Figure 2 – Populated Circuit Board Photograph, Bottom.
# 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{IN}$</td>
<td>30</td>
<td>800</td>
<td>1200</td>
<td>VDC</td>
<td>For Electric Vehicle Emergency PSU.</td>
</tr>
<tr>
<td><strong>Maximum Output Power</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{OUT}$</td>
<td>$P_{OUT}$</td>
<td>2.2</td>
<td>W</td>
<td>2.2</td>
<td>W</td>
<td>$V_{IN}$ of 30 VDC, $P_{MAX} &lt; 0.75$ W for Start-up, $P_{MAX} &lt; 2.2$ W for Reducing Input Voltage</td>
</tr>
<tr>
<td>$P_{OUT}$</td>
<td>$P_{OUT}$</td>
<td>15</td>
<td>W</td>
<td>15</td>
<td>W</td>
<td>$V_{IN}$ of 60 VDC to 1200 VDC.</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{OUT}$</td>
<td>12</td>
<td>V</td>
<td>12</td>
<td>V</td>
<td>$\pm 5%$ ($V_{IN} &gt; 400$ VDC).</td>
</tr>
<tr>
<td>Output Current</td>
<td>$I_{OUT}$</td>
<td>1.25</td>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Ripple Voltage</td>
<td>$V_{RIPPLE}$</td>
<td>300</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Isolation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Meets IEC 60664-1 as a Minimum. Reinforce Better.</td>
</tr>
<tr>
<td><strong>Ambient Temperature</strong></td>
<td>$T_{AMB}$</td>
<td>-40</td>
<td>°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3 Schematic

Figure 3 – Schematic.
4 Circuit Description

4.1 INN3996CQ IC Primary

One end of the transformer primary is connected to the DC bus. The other is connected to a high-voltage (800 V) MOSFET (Q1) that is a cascode connected to the Drain of the integrated power MOSFET inside the INN3996CQ IC (U1). In this configuration the effective Drain-Source voltage rating of the primary is 1700 V<sub>PK</sub>.

High-voltage ceramic capacitors C1 and C2 are used for the decoupling capacitor for the DC input voltage, and a low cost RCD clamp formed by D1, D3, R4, R1, R2 and C3 limits the peak total drain voltage, which is the sum of STACKFET and INN3996CQ drain voltages, to about 1460 V at 1200 VDC input due to the effects of transformer leakage inductance. Capacitor C7, Y capacitor, is used to attenuate the high frequency common mode noise on the output.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C6, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C4, and fed in the BPP pin via a current limiting resistor R3.

Zener diode VR1 and VR2 clamp the maximum drain-source voltage across the INN3997CQ IC (U1) to below 800 V. Zener diode VR3 ensures that the maximum gate-source voltage of Q1 does not exceed 15 V. Resistor R6, R7, and C5 provide bias to enhance the gate of Q1 when its source is switched low by the drain of U1.

4.2 INN3996CQ IC Secondary

The secondary-side of the INN3996CQ IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 12 V output is provided by SR FETs Q2 and Q3. Low ESR capacitors, C11, C12, C13, C16, C17 and output inductor L1 provide filtering. RC snubber network comprising R9, R10, and C8 for Q2 and Q3 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gates of Q2 and Q3 are turned on based on the winding voltage sensed via R8 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the
device, fed into the VO pin. It will charge the decoupling capacitor C10 via an internal regulator.

Resistors R12 and R13 form a voltage divider network that senses the output voltage. INN3996CQ IC has an internal reference of 1.265 V. Capacitor C14 provides decoupling from high frequency noise affecting power supply operation, and C15 and R14 is the feedforward network to speed up the response time to lower the output ripple. The output current is sensed by R11 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.
5 PCB Layout

Layers: 4
Board Thickness: 0.062”
Board Material: FR4
Copper Weight: 2 oz
Surface finish: LF HASL

Figure 4 – Printed Circuit Board Layout (Top).

Figure 5 – Printed Circuit Board Layout (Bottom).
Figure 6 – Printed Circuit Board Layout (Internal layer 1).

Figure 7 – Printed Circuit Board Layout (Internal layer 2).
## 6 Bill of Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Qty</th>
<th>Ref Des</th>
<th>Description</th>
<th>Mfg Part Number</th>
<th>Mfg</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2</td>
<td>C1 C2</td>
<td>0.047 µF, ±10%, 1000 V (1kV), Ceramic, X7R, 1812</td>
<td></td>
<td>1812Y1K00473KST</td>
<td>Knowles Syfer</td>
</tr>
<tr>
<td>2 1</td>
<td>C3</td>
<td>470 pF, ±10%, 1000 V (1kV), Ceramic, X7R, 1206</td>
<td></td>
<td>C1206C472KDRACAUTO</td>
<td>Kemet</td>
</tr>
<tr>
<td>3 4</td>
<td>C4</td>
<td>22 µF ±20%, 25V Ceramic X5R 0805</td>
<td></td>
<td>GRT21BR61E226ME13L</td>
<td>Murata</td>
</tr>
<tr>
<td>4 2</td>
<td>C5</td>
<td>20 pF, ±5%, 1000 V (1kV), Ceramic, C0G, NPO, 1206</td>
<td></td>
<td>C1206C202JDGACAUTO</td>
<td>Kemet</td>
</tr>
<tr>
<td>5 1</td>
<td>C6</td>
<td>0.47 µF, ±10%, 50 V, Ceramic, X7R, 0805, -55°C ~ 125°C</td>
<td></td>
<td>CGA4J3X7R1H474K125AB</td>
<td>TDK</td>
</tr>
<tr>
<td>6 1</td>
<td>C7</td>
<td>220 pF, ±20%, 760 VAC, Ceramic Y5U (E) Radial, Disc</td>
<td></td>
<td>AY1222M475UC63L0</td>
<td>Vishay</td>
</tr>
<tr>
<td>1 7</td>
<td>C8</td>
<td>2200 pF, ±20%, 760 VAC, Ceramic Y5U (E) Radial, Disc</td>
<td></td>
<td>AY1222M475UC63L0</td>
<td>Vishay</td>
</tr>
<tr>
<td>1 8</td>
<td>C9</td>
<td>50 V, Ceramic, X7R, 0805</td>
<td></td>
<td>GCTM31A5C2J391JX01D</td>
<td>Murata</td>
</tr>
<tr>
<td>8 2</td>
<td>C10</td>
<td>2200 pF, ±20%, 760 VAC, Ceramic Y5U (E) Radial, Disc</td>
<td></td>
<td>AY1222M475UC63L0</td>
<td>Vishay</td>
</tr>
<tr>
<td>1 9</td>
<td>C14</td>
<td>1MΩ, ±1%, 1/8 W, Thick Film, 0805</td>
<td></td>
<td>TRM31A5C2J391JX01D</td>
<td>Murata</td>
</tr>
<tr>
<td>10 3</td>
<td>C11 C12</td>
<td>220 µF, 25 V, Electrolytic, 0.260&quot; L x 0.260&quot; W (6.60 mm x 6.60 mm) x 0.315&quot; H (8.00 mm), SMD</td>
<td></td>
<td>EMZR250ARA221MF80G</td>
<td>United Chemi-Con</td>
</tr>
<tr>
<td>10 2</td>
<td>C17</td>
<td>100 µF, ±20%, 25 V, Z=320 mΩ, Electrolytic, 0.260&quot; L x 0.260&quot; W (6.60 mm x 6.60 mm) x 0.315&quot; H (8.00 mm), SMD</td>
<td></td>
<td>UCD1E101MCL1GS</td>
<td>Nichicon</td>
</tr>
<tr>
<td>15 2</td>
<td>D1 D3</td>
<td>Diode Standard 1000 V 1 A SMT DO-214AC (SMA)</td>
<td></td>
<td>USIMHE3_A/I</td>
<td>Vishay</td>
</tr>
<tr>
<td>16 2</td>
<td>D2 D4</td>
<td>Diode, General Purpose, 250 V, 200 mA, SC-76, SOD-323</td>
<td></td>
<td>NSVBAS21AHT1G</td>
<td>ON Semi</td>
</tr>
<tr>
<td>17 2</td>
<td>L1</td>
<td>1.5 µH, ±1%, Shielded, Wirewound, Inductor, 4.5 A, 42 mΩ Max, Automotive, AEC-Q200, 2-SMD</td>
<td></td>
<td>SRP4020TA-1R5M</td>
<td>Bourns</td>
</tr>
<tr>
<td>18 2</td>
<td>Q1</td>
<td>MOSFET, N-Channel 800V 0.2A (Tc) 125 W (Tc) SMT D2PAK</td>
<td></td>
<td>SL2605NDR-80125</td>
<td>STMicro</td>
</tr>
<tr>
<td>19 2</td>
<td>Q2 Q3</td>
<td>MOSFET, N-Channel, 200 V, 13 A (Tc), 68W (Tc), Automotive, AEC-Q101, PowerPAK® SO-8, PowerPAK SO-8</td>
<td></td>
<td>SQA4G4EP-T1_GE3</td>
<td>Vishay</td>
</tr>
<tr>
<td>20 2</td>
<td>R1 R2</td>
<td>RES, 1.0 MΩ, 1%, 1/4 W, Thick Film, 1206</td>
<td></td>
<td>ERJ-8ENF1004V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>21 1</td>
<td>R3</td>
<td>21.0 kΩ, 1%, 1/8 W, Thick Film, 0805</td>
<td></td>
<td>ERJ-6ENF2102V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>21 1</td>
<td>R4</td>
<td>RES, 39 Ω, 5%, 1/4 W, Thick Film, 1206</td>
<td></td>
<td>ERJ-8GEY390V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>21 1</td>
<td>R5</td>
<td>RES, 10 Ω, 5%, 1/4 W, Thick Film, 1206</td>
<td></td>
<td>ERJ-8GEY100V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>21 2</td>
<td>R6 R7</td>
<td>RES, 1.0 MΩ, 5%, 1/4 W, Thick Film, 1206</td>
<td></td>
<td>ERJ-8GEY105V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>22 1</td>
<td>R8</td>
<td>RES, 100 Ω, 1%, 1/4 W, Thick Film, 1206</td>
<td></td>
<td>ERJ-8ENF1000V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>22 2</td>
<td>R9 R10</td>
<td>RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206</td>
<td></td>
<td>ERJ-8GEY510V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>23 1</td>
<td>R11</td>
<td>0.011 Ω, ±1%, ±75ppm/°C, 1 W, 1206, Automotive AEC-Q200, 2-SMD, Current Sense, -55°C ~ 155°C</td>
<td></td>
<td>ERJ-6CWF011V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>23 1</td>
<td>R12</td>
<td>RES, 11.8 kΩ, 1%, 1/8 W, Thick Film, 0805</td>
<td></td>
<td>ERJ-8ENF1182V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>23 1</td>
<td>R13</td>
<td>RES, 100 kΩ, 1%, 1/8 W, Thick Film, 0805</td>
<td></td>
<td>ERJ-8ENF1003V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>23 1</td>
<td>R14</td>
<td>RES, 15 kΩ, 5%, 1/8 W, Thick Film, 0805</td>
<td></td>
<td>ERJ-9GEYJ515V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>24 1</td>
<td>T1</td>
<td>4700 pF, ±10%, 1000 V (1kV), Ceramic, X7R, 1206</td>
<td></td>
<td>C1206C472KDRACAUTO</td>
<td>Kemet</td>
</tr>
<tr>
<td>24 1</td>
<td>T1</td>
<td>Bobbin, EQ25, 4 pins, 3pri, 0sec</td>
<td></td>
<td>EQ-2506</td>
<td>Shen Zhen Xin Yu Jia Tech</td>
</tr>
<tr>
<td>25 1</td>
<td>VR1 VR2</td>
<td>TVS DIODE, 482 V Clamp, 1.3A Ipp, SMT, DO-214AA (SMBJ)</td>
<td></td>
<td>TPSM6550A-A</td>
<td>Littlefuse</td>
</tr>
<tr>
<td>25 1</td>
<td>VR3</td>
<td>Zener Diode, 15 V, 500 mW, ±5%, SMD, SOD-123</td>
<td></td>
<td>MMSZ5245B-8-18</td>
<td>Vishay</td>
</tr>
</tbody>
</table>
7 Transformer Design

7.1 Electrical Diagram

![Electrical Diagram](image)

**Figure 8** – Electrical Diagram.

7.2 Electrical Specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Spec.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Primary Inductance</td>
<td>Measured at 1 V&lt;sub&gt;PK-PK&lt;/sub&gt;, 100 kHz switching frequency, between pin 3 and 4, with all other windings open.</td>
<td>1187 μH ±5%</td>
</tr>
<tr>
<td>Resonant Frequency</td>
<td>Between pin 3 and 4, other windings open.</td>
<td>1,200 kHz (Min.)</td>
</tr>
<tr>
<td>Primary Leakage Inductance</td>
<td>Between pin 3 and 4, with pins: FL1-FL2 shorted.</td>
<td>7.0 μH (Max.)</td>
</tr>
</tbody>
</table>

7.3 Transformer Build Diagram

![Transformer Build Diagram](image)

**Figure 9** – Transformer Build Diagram.
7.4 **Material List**

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[8]</td>
<td>Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 27.5 mm x 52 mm.</td>
</tr>
</tbody>
</table>

7.5 **Transformer Instruction**

- **Winding Preparation**
  - Make 2 slots with 2 mm width on flanges of secondary side of bobbin Item [2], (see illustration below). Position the bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.

- **WD1 1st Primary**
  - Start at pin 4, wind 25 turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, leave this wire with enough length for WD4 – 2nd Primary.
  - Insulation
    - 1 layer of tape Item [7].

- **WD2: Bias**
  - Start at pin1, wind 6 bifilar turns of wire Item [4] from left to right, spread wires evenly on the bobbin. At the last turn bring the wires back to the left and terminate at pin 2.
  - Insulation
    - 1 layer of tape Item [7].

- **WD3 Secondary**
  - Start at left slot of secondary side of bobbin, use wire Item [5] leaving ~ 1”, mark as FL1, and wind 5 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~ 1” and mark as FL2.
  - Repeat same winding above and on top, also start as FL1 and end FL2.
  - Insulation
    - 1 layer of tape Item [7].

- **WD4 2nd Primary**
  - Using wire floating from WD1, continue winding 25 turns in 2 layers, and terminate at pin 3.
  - Insulation
    - Place 1 layer of tape Item [7], bring 2 wires floating FL1 from Secondary – WD3 to right slot and continue placing another 2 layers of tape to secure these wires and all the windings.

- **Finish Assembly**
  - Gap core halves to get 1187 µH. Use 50 mm of bus wire Item [6], solder to pin 2 then lean along core halves and secure with tape. Varnish with Item [9]. Places 2 layers of tape Item [8] at bottom of transformer, wrap up to the body, and 1 layer of tape Item [7] around the transformer, (see illustration below).
7.6 **Winding Illustrations**

**Winding Preparation**

Make 2 slots with 2 mm width on flanges of secondary side of bobbin Item [2], (see illustration beside). Position the bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.

**WD1 1st Primary**

Start at pin 4, wind 25 turns of wire Item [3] in 2 layers, with tight tension, from left to right and right to left. At the last turn, leave this wire with enough length for WD4 – 2nd Primary.
<table>
<thead>
<tr>
<th><strong>Insulation</strong></th>
<th>1 layer of tape Item [7].</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>WD2: Bias</strong></td>
<td>Start at pin1, wind 6 bifilar turns of wire Item [4] from left to right, spread wires evenly on the bobbin. At the last turn bring the wires back to the left and terminate at pin 2.</td>
</tr>
<tr>
<td>Insulation</td>
<td>1 layer of tape item [7].</td>
</tr>
<tr>
<td>------------------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>WD3 Secondary</td>
<td></td>
</tr>
<tr>
<td>Start at left slot of secondary side of bobbin, use wire Item [5] leaving ~ 1”, mark as FL1, and wind 5 turns with tight tension. At the last turn, exit the wire at the right slot, also leaving ~ 1” and mark as FL2. Repeat same winding above and on top, also start as FL1 and end FL2.</td>
<td></td>
</tr>
</tbody>
</table>
Insulation

1 layer of tape Item [7].

WD4 2\textsuperscript{nd} Primary

Using wire floating from WD1, continue winding 25 turns in 2 layers, and terminate at pin 3.
Place 1 layer of tape Item [7], bring 2 wires floating FL1 from Secondary – WD3 to right slot and continue placing another 2 layers of tape to secure these wires and all the windings.
Finish

Gap core halves to get 1187 µH. Use 50 mm of bus wire Item [6], solder to pin 2 then lean along core halves and secure with tape. Varnish with Item [9].

Finish (Cont’d)

Places 2 layers of tape Item [8] at bottom of transformer, wrap up to the body, and 1 layer of tape Item [7] around the transformer, (see illustration below).
8 Performance Data
All measurements performed with room ambient temperature. Measured at PCB output terminal.

8.1 Efficiency vs. Load and Input Voltage

Figure 10 – Efficiency vs. Load and Input Voltage, Room Temperature.
8.2 Full Load Efficiency vs. Line

![Graph showing efficiency vs. line voltage](image-url)

**Figure 11** – Efficiency vs. Line (VDC), Room Temperature.
8.3 **Efficiency at Low Input Voltage**

<table>
<thead>
<tr>
<th>$V_{IN}$ (VDC)</th>
<th>$P_{IN}$ (W)</th>
<th>$V_{OUT}$ (V)</th>
<th>$I_{OUT}$ (A)</th>
<th>$P_{OUT}$ (W)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>130</td>
<td>16.97</td>
<td>12.03</td>
<td>1.25</td>
<td>15.03</td>
<td>88.60</td>
</tr>
<tr>
<td>100</td>
<td>17.14</td>
<td>12</td>
<td>1.25</td>
<td>14.99</td>
<td>87.45</td>
</tr>
<tr>
<td>90</td>
<td>17.32</td>
<td>12.01</td>
<td>1.25</td>
<td>15.00</td>
<td>86.63</td>
</tr>
<tr>
<td>60</td>
<td>17.14</td>
<td>11.53</td>
<td>1.25</td>
<td>14.41</td>
<td>84.29</td>
</tr>
<tr>
<td>40</td>
<td>9.98</td>
<td>11.42</td>
<td>0.70</td>
<td>7.99</td>
<td>80.13</td>
</tr>
<tr>
<td>35</td>
<td>8.02</td>
<td>11.40</td>
<td>0.55</td>
<td>6.27</td>
<td>78.10</td>
</tr>
<tr>
<td>30</td>
<td>2.84</td>
<td>11.59</td>
<td>0.19</td>
<td>2.20</td>
<td>77.38</td>
</tr>
</tbody>
</table>

Note: 2 W Load at 30 VDC Input during power down only.

8.4 **No-Load Input Power**

**Figure 12** – No-Load Input Power, Room Temperature.
8.5 **Load and Line Regulation**

Measurements taken at 0% to 100% of rated load

![Graph showing Load and Line Regulation](image)

**Figure 13** – Output Voltage vs. Output Current and Input Voltage (VDC), Room Temperature.
9 Waveforms

9.1 INN3996CQ Drain Voltage and Current, Steady-State

**Figure 14** – Drain Voltage and Current Waveforms. 
\[V_{IN} = 400 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A}, \]
\[V_{DS(MAX)} = 604 \text{ V}.\]  
Upper: \(V_{DRAIN}\), 300 V, 400 \(\mu\)s / div.  
Lower: \(I_{DRAIN}\), 500 mA, 400 \(\mu\)s / div.  
Bottom Half: Zoom @ 10 \(\mu\)s / div.

**Figure 15** – Drain Voltage and Current Waveforms. 
\[V_{IN} = 800 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A}, \]
\[V_{DS(MAX)} = 782 \text{ V}.\]  
Upper: \(V_{DRAIN}\), 300 V, 400 \(\mu\)s / div.  
Lower: \(I_{DRAIN}\), 500 mA, 400 \(\mu\)s / div.  
Bottom Half: Zoom @ 10 \(\mu\)s / div.

**Figure 16** – Drain Voltage and Current Waveforms. 
\[V_{IN} = 1000 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A}, \]
\[V_{DS(MAX)} = 782 \text{ V}.\]  
Upper: \(V_{DRAIN}\), 300 V, 400 \(\mu\)s / div.  
Lower: \(I_{DRAIN}\), 500 mA, 400 \(\mu\)s / div.  
Bottom Half: Zoom @ 10 \(\mu\)s / div.

**Figure 17** – Drain Voltage and Current Waveforms. 
\[V_{IN} = 1200 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A}, \]
\[V_{DS(MAX)} = 782 \text{ V}.\]  
Upper: \(V_{DRAIN}\), 300 V, 400 \(\mu\)s / div.  
Lower: \(I_{DRAIN}\), 500 mA, 400 \(\mu\)s / div.  
Bottom Half: Zoom @ 10 \(\mu\)s / div.
9.2 **INN3996CQ Drain Voltage and Current, Start-up**

**Figure 18** – Drain Voltage and Current Waveforms.
- $V_{IN} = 400 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
- $V_{DS(MAX)} = 604 \text{ V}$.
  - Upper: $V_{DRAIN}$, 300 V, 200 ms / div.
  - Lower: $I_{DRAIN}$, 500 mA, 200 ms / div.

**Figure 19** – Drain Voltage and Current Waveforms.
- $V_{IN} = 800 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
- $V_{DS(MAX)} = 770 \text{ V}$.
  - Upper: $V_{DRAIN}$, 300 V, 200 ms / div.
  - Lower: $I_{DRAIN}$, 500 mA, 200 ms / div.

**Figure 20** – Drain Voltage and Current Waveforms.
- $V_{IN} = 1000 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
- $V_{DS(MAX)} = 782 \text{ V}$.
  - Upper: $V_{DRAIN}$, 300 V, 200 ms / div.
  - Lower: $I_{DRAIN}$, 500 mA, 200 ms / div.

**Figure 21** – Drain Voltage and Current Waveforms.
- $V_{IN} = 1200 \text{ VDC}$, $I_{OUT} = 1.25 \text{ A}$.
- $V_{DS(MAX)} = 782 \text{ V}$.
  - Upper: $V_{DRAIN}$, 300 V, 200 ms / div.
  - Lower: $I_{DRAIN}$, 500 mA, 200 ms / div.
9.3 **Total and StackFET Drain to Source Voltage, Steady-State**

**Figure 22** – Total and STACKFET Drain to Source Voltage Waveforms.
- $V_{IN} = 400$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 65$ V, $V_{DS\ TOTAL(MAX)} = 652$ V.
- Upper: $V_{TOTAL}$, 500 V, 400 $\mu$s / div.
- Lower: $V_{STACKFET}$, 200 V, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 23** – Total and STACKFET Drain to Source Voltage Waveforms.
- $V_{IN} = 800$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 278$ V, $V_{TOTAL(MAX)} = 1047$ V.
- Upper: $V_{TOTAL}$, 500 V, 400 $\mu$s / div.
- Lower: $V_{STACKFET}$, 200 V, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 24** – Total and STACKFET Drain to Source Voltage Waveforms.
- $V_{IN} = 1000$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 476$ V, $V_{TOTAL(MAX)} = 1265$ V.
- Upper: $V_{TOTAL}$, 500 V, 400 $\mu$s / div.
- Lower: $V_{STACKFET}$, 200 V, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 25** – Total and STACKFET Drain to Source Voltage Waveforms.
- $V_{IN} = 1200$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 674$ V, $V_{TOTAL(MAX)} = 1463$ V.
- Upper: $V_{TOTAL}$, 500 V, 400 $\mu$s / div.
- Lower: $V_{STACKFET}$, 200 V, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.
Total and StackFET Drain to Source Voltage, Start-up

**Figure 26** – Total and STACKFET Drain to Source Voltage Waveforms.
- $V_{IN} = 400$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 81$ V, $V_{DS,TOTAL(MAX)} = 672$ V.
- Upper: $V_{TOTAL}$, 500 V, 200 ms / div.
- Lower: $V_{STACKFET}$, 200 V, 200 ms / div.

**Figure 27** – Total and STACKFET Drain to Source Voltage Waveforms.
- $V_{IN} = 800$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 294$ V, $V_{TOTAL(MAX)} = 1047$ V.
- Upper: $V_{TOTAL}$, 500 V, 200 ms / div.
- Lower: $V_{STACKFET}$, 200 V, 200 ms / div.

**Figure 28** – Total and StackFET Drain to Source Voltage Waveforms.
- $V_{IN} = 1000$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 500$ V, $V_{TOTAL(MAX)} = 1265$ V.
- Upper: $V_{TOTAL}$, 500 V, 200 ms / div.
- Lower: $V_{STACKFET}$, 200 V, 200 ms / div.

**Figure 29** – Total and STACKFET Drain to Source Voltage Waveforms.
- $V_{IN} = 1200$ VDC, $I_{OUT} = 1.25$ A.
- $V_{STACKFET(MAX)} = 697$ V, $V_{TOTAL(MAX)} = 1463$ V.
- Upper: $V_{TOTAL}$, 500 V, 200 ms / div.
- Lower: $V_{STACKFET}$, 200 V, 200 ms / div.
9.5 **SR FET Waveforms, Steady-State**

**Figure 30** – SR FET Drain to Source Voltage Waveforms.

- $V_{IN} =$ 400 VDC, $I_{OUT} =$ 1.25 A.
- SRFET $V_{DS(MAX)} =$ 57.3 V.
- SRFET $I_{DS(MAX)} =$ 13.3 A.
- Upper: SRFET $V_{DS}$, 50 V, 400 $\mu$s / div.
- Lower: SRFET $I_{DS}$, 5 A, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 31** – SR FET Drain to Source Voltage Waveforms.

- $V_{IN} =$ 800 VDC, $I_{OUT} =$ 1.25 A.
- SRFET $V_{DS(MAX)} =$ 96.8 V.
- SRFET $I_{DS(MAX)} =$ 13.1 A.
- Upper: SRFET $V_{DS}$, 50 V, 400 $\mu$s / div.
- Lower: SRFET $I_{DS}$, 5 A, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 32** – SR FET Drain to Source Voltage Waveforms.

- $V_{IN} =$ 1000 VDC, $I_{OUT} =$ 1.25 A.
- SRFET $V_{DS(MAX)} =$ 118.6 V.
- SRFET $I_{DS(MAX)} =$ 13.3 A.
- Upper: SRFET $V_{DS}$, 50 V, 400 $\mu$s / div.
- Lower: SRFET $I_{DS}$, 5 A, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 33** – SR FET Drain to Source Voltage Waveforms.

- $V_{IN} =$ 1200 VDC, $I_{OUT} =$ 1.25 A.
- SRFET $V_{DS(MAX)} =$ 138.3 V.
- SRFET $I_{DS(MAX)} =$ 13.7 A.
- Upper: SRFET $V_{DS}$, 50 V, 400 $\mu$s / div.
- Lower: SRFET $I_{DS}$, 5 A, 400 $\mu$s / div.
- Bottom Half: Zoom @ 10 $\mu$s / div.
9.6 **SR FET Waveforms, Start-up**

**Figure 34** – SRFET Drain to Source Voltage Waveforms.
- $V_{IN} = 400$ VDC, $I_{OUT} = 1.25$ A.
- SRFET $V_{DS(MAX)} = 57.3$ V.
- SRFET $I_{DS(MAX)} = 13.3$ A.
- Upper: SRFET $V_{DS}$, 50 V, 200 ms / div.
- Lower: SRFET $I_{DS}$, 5 A, 200 ms / div.

**Figure 35** – SRFET Drain to Source Voltage Waveforms.
- $V_{IN} = 800$ VDC, $I_{OUT} = 1.25$ A.
- SRFET $V_{DS(MAX)} = 98.8$ V.
- SRFET $I_{DS(MAX)} = 13.5$ A.
- Upper: SRFET $V_{DS}$, 50 V, 200 ms / div.
- Lower: SRFET $I_{DS}$, 5 A, 200 ms / div.

**Figure 36** – SRFET Drain to Source Voltage Waveforms.
- $V_{IN} = 1000$ VDC, $I_{OUT} = 1.25$ A.
- SRFET $V_{DS(MAX)} = 118.6$ V.
- SRFET $I_{DS(MAX)} = 13.5$ A.
- Upper: SRFET $V_{DS}$, 50 V, 200 ms / div.
- Lower: SRFET $I_{DS}$, 5 A, 200 ms / div.

**Figure 37** – SRFET Drain to Source Voltage Waveforms.
- $V_{IN} = 1200$ VDC, $I_{OUT} = 1.25$ A.
- SRFET $V_{DS(MAX)} = 140.3$ V.
- SRFET $I_{DS(MAX)} = 13.7$ A.
- Upper: SRFET $V_{DS}$, 50 V, 200 ms / div.
- Lower: SRFET $I_{DS}$, 5 A, 200 ms / div.
9.7 **Output Ripple Measurements**

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor includes one (1) 1 \( \mu \)F/50 V ceramic type.

![Probe Ground](image1)

![Probe Tip](image2)

**Figure 38** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

**Figure 39** – Oscilloscope Probe with Probe Master ([www.probemaster.com](http://www.probemaster.com)) 4987A BNC Adapter. (Modified with wires for ripple measurement, and one parallel decoupling capacitor added)
9.7.1 100% Loading Condition

**Figure 40** – Output Voltage Ripple.
\[ V_{\text{IN}} = 400 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} \) / div.
\( V_{\text{RIPPLE}} = 168 \text{ mV}_{\text{P-P}}. \)

**Figure 41** – Output Voltage Ripple.
\[ V_{\text{IN}} = 800 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} \) / div.
\( V_{\text{RIPPLE}} = 182 \text{ mV}_{\text{P-P}}. \)

**Figure 42** – Output Voltage Ripple.
\[ V_{\text{IN}} = 1000 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} \) / div.
\( V_{\text{RIPPLE}} = 194 \text{ mV}_{\text{P-P}}. \)

**Figure 43** – Output Voltage Ripple.
\[ V_{\text{IN}} = 1200 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} \) / div.
\( V_{\text{RIPPLE}} = 204 \text{ mV}_{\text{P-P}}. \)
9.7.2 75% Loading Condition

**Figure 44** – Output Voltage Ripple.
\[ V_{\text{IN}} = 400 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \[ V_{\text{OUT}}, \quad 50 \text{ mV}, \quad 5.6 \text{ ms} / \text{div}. \]
Lower: Zoom @ 40 µs / div.
\[ V_{\text{RIPPLE}} = 160 \text{ mV}_{\text{P-P}}. \]

**Figure 45** – Output Voltage Ripple.
\[ V_{\text{IN}} = 800 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \[ V_{\text{OUT}}, \quad 50 \text{ mV}, \quad 5.6 \text{ ms} / \text{div}. \]
Lower: Zoom @ 40 µs / div.
\[ V_{\text{RIPPLE}} = 176 \text{ mV}_{\text{P-P}}. \]

**Figure 46** – Output Voltage Ripple.
\[ V_{\text{IN}} = 1000 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \[ V_{\text{OUT}}, \quad 50 \text{ mV}, \quad 5.6 \text{ ms} / \text{div}. \]
Lower: Zoom @ 40 µs / div.
\[ V_{\text{RIPPLE}} = 178 \text{ mV}_{\text{P-P}}. \]

**Figure 47** – Output Voltage Ripple.
\[ V_{\text{IN}} = 1200 \text{ VDC}, \quad I_{\text{OUT}} = 1.25 \text{ A}. \]
Upper: \[ V_{\text{OUT}}, \quad 50 \text{ mV}, \quad 5.6 \text{ ms} / \text{div}. \]
Lower: Zoom @ 40 µs / div.
\[ V_{\text{RIPPLE}} = 182 \text{ mV}_{\text{P-P}}. \]
9.7.3 50% Loading Condition

**Figure 48** – Output Voltage Ripple.
\[ V_{IN} = 400 \text{ VDC, } I_{OUT} = 1.25 \text{ A.} \]
Upper: \( V_{OUT} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} / \text{div.} \)
\[ V_{RIPPLE} = 140 \text{ mV}_{\text{P-P}}. \]

**Figure 49** – Output Voltage Ripple.
\[ V_{IN} = 800 \text{ VDC, } I_{OUT} = 1.25 \text{ A.} \]
Upper: \( V_{OUT} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} / \text{div.} \)
\[ V_{RIPPLE} = 138 \text{ mV}_{\text{P-P}}. \]

**Figure 50** – Output Voltage Ripple.
\[ V_{IN} = 1000 \text{ VDC, } I_{OUT} = 1.25 \text{ A.} \]
Upper: \( V_{OUT} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} / \text{div.} \)
\[ V_{RIPPLE} = 144 \text{ mV}_{\text{P-P}}. \]

**Figure 51** – Output Voltage Ripple.
\[ V_{IN} = 1200 \text{ VDC, } I_{OUT} = 1.25 \text{ A.} \]
Upper: \( V_{OUT} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \text{s} / \text{div.} \)
\[ V_{RIPPLE} = 174 \text{ mV}_{\text{P-P}}. \]
9.7.4 25% Loading Condition

Figure 52 – Output Voltage Ripple.
\( V_{\text{IN}} = 400 \, \text{VDC}, \, I_{\text{OUT}} = 1.25 \, \text{A}. \)
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \)s / div.
\( V_{\text{RIPPLE}} = 99 \, \text{mV}_{\text{P-P}}. \)

Figure 53 – Output Voltage Ripple.
\( V_{\text{IN}} = 800 \, \text{VDC}, \, I_{\text{OUT}} = 1.25 \, \text{A}. \)
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \)s / div.
\( V_{\text{RIPPLE}} = 111 \, \text{mV}_{\text{P-P}}. \)

Figure 54 – Output Voltage Ripple.
\( V_{\text{IN}} = 1000 \, \text{VDC}, \, I_{\text{OUT}} = 1.25 \, \text{A}. \)
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \)s / div.
\( V_{\text{RIPPLE}} = 126 \, \text{mV}_{\text{P-P}}. \)

Figure 55 – Output Voltage Ripple.
\( V_{\text{IN}} = 1200 \, \text{VDC}, \, I_{\text{OUT}} = 1.25 \, \text{A}. \)
Upper: \( V_{\text{OUT}} \), 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 \( \mu \)s / div.
\( V_{\text{RIPPLE}} = 174 \, \text{mV}_{\text{P-P}}. \)
9.7.5 0% Loading Condition

**Figure 56** – Output Voltage Ripple.
$V_{IN} = 400$ VDC, $I_{OUT} = 1.25$ A.
Upper: $V_{OUT}$, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
$V_{RIPPLE} = 67$ mV_{P-P}.

**Figure 57** – Output Voltage Ripple.
$V_{IN} = 800$ VDC, $I_{OUT} = 1.25$ A.
Upper: $V_{OUT}$, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
$V_{RIPPLE} = 91$ mV_{P-P}.

**Figure 58** – Output Voltage Ripple.
$V_{IN} = 1000$ VDC, $I_{OUT} = 1.25$ A.
Upper: $V_{OUT}$, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
$V_{RIPPLE} = 103$ mV_{P-P}.

**Figure 59** – Output Voltage Ripple.
$V_{IN} = 1200$ VDC, $I_{OUT} = 1.25$ A.
Upper: $V_{OUT}$, 50 mV, 5.6 ms / div.
Lower: Zoom @ 40 µs / div.
$V_{RIPPLE} = 115$ mV_{P-P}.
Output Voltage Ripple (ATE)

Figure 60 – Output Voltage Ripple.
9.9 **Output Load Transient**

9.9.1 Output Load Transient, 100% to 50% Load

**Figure 61** – Output Load Transient, 100% to 50% Load.
\[
\begin{align*}
V_{\text{IN}} &= 400 \text{ VDC}, I_{\text{OUT}} = 1.25 \text{ A to 0.625 A}. \\
V_{\text{OUT(MAX)}} &= 12.31 \text{ V}, V_{\text{OUT(MIN)}} = 11.91 \text{ V}. \\
\text{Upper: } V_{\text{OUT}}, 400 \text{ mV, 50 ms / div}. \\
\text{Lower: } I_{\text{OUT}}, 1 \text{ A, 50 ms / div}. 
\end{align*}
\]

**Figure 62** – Output Load Transient, 100% to 50% Load.
\[
\begin{align*}
V_{\text{IN}} &= 800 \text{ VDC}, I_{\text{OUT}} = 1.25 \text{ A to 0.625 A}. \\
V_{\text{OUT(MAX)}} &= 12.34 \text{ V}, V_{\text{OUT(MIN)}} = 11.85 \text{ V}. \\
\text{Upper: } V_{\text{OUT}}, 400 \text{ mV, 50 ms / div}. \\
\text{Lower: } I_{\text{OUT}}, 1 \text{ A, 50 ms / div}. 
\end{align*}
\]

**Figure 63** – Output Load Transient, 100% to 50% Load.
\[
\begin{align*}
V_{\text{IN}} &= 1000 \text{ VDC}, I_{\text{OUT}} = 1.25 \text{ A to 0.625 A}. \\
V_{\text{OUT(MAX)}} &= 12.34 \text{ V}, V_{\text{OUT(MIN)}} = 11.85 \text{ V}. \\
\text{Upper: } V_{\text{OUT}}, 400 \text{ mV, 50 ms / div}. \\
\text{Lower: } I_{\text{OUT}}, 1 \text{ A, 50 ms / div}. 
\end{align*}
\]

**Figure 64** – Output Load Transient, 100% to 50% Load.
\[
\begin{align*}
V_{\text{IN}} &= 1200 \text{ VDC}, I_{\text{OUT}} = 1.25 \text{ A to 0.625 A}. \\
V_{\text{OUT(MAX)}} &= 12.29 \text{ V}, V_{\text{OUT(MIN)}} = 11.82 \text{ V}. \\
\text{Upper: } V_{\text{OUT}}, 400 \text{ mV, 50 ms / div}. \\
\text{Lower: } I_{\text{OUT}}, 1 \text{ A, 50 ms / div}. 
\end{align*}
\]
9.9.2 Output Load Transient, 100% to 0% Load

**Figure 65** – Output Load Transient, 100% to 0% Load.
\[ V_{IN} = 400 \text{ VDC}, \quad I_{OUT} = 1.25 \text{ A to 0 A}. \]
\[ V_{OUT(MAX)} = 12.29 \text{ V}, \quad V_{OUT(MIN)} = 11.8 \text{ V}. \]
Upper: \( V_{OUT} \), 400 mV, 50 ms / div.
Lower: \( I_{OUT} \), 1 A, 50 ms / div.

**Figure 66** – Output Load Transient, 100% to 0% Load.
\[ V_{IN} = 800 \text{ VDC}, \quad I_{OUT} = 1.25 \text{ A to 0 A}. \]
\[ V_{OUT(MAX)} = 12.34 \text{ V}, \quad V_{OUT(MIN)} = 11.77 \text{ V}. \]
Upper: \( V_{OUT} \), 400 mV, 50 ms / div.
Lower: \( I_{OUT} \), 1 A, 50 ms / div.

**Figure 67** – Output Load Transient, 100% to 0% Load.
\[ V_{IN} = 1000 \text{ VDC}, \quad I_{OUT} = 1.25 \text{ A to 0 A}. \]
\[ V_{OUT(MAX)} = 12.29 \text{ V}, \quad V_{OUT(MIN)} = 11.77 \text{ V}. \]
Upper: \( V_{OUT} \), 400 mV, 50 ms / div.
Lower: \( I_{OUT} \), 1 A, 50 ms / div.

**Figure 68** – Output Load Transient, 100% to 0% Load.
\[ V_{IN} = 1200 \text{ VDC}, \quad I_{OUT} = 1.25 \text{ A to 0 A}. \]
\[ V_{OUT(MAX)} = 12.37 \text{ V}, \quad V_{OUT(MIN)} = 11.74 \text{ V}. \]
Upper: \( V_{OUT} \), 400 mV, 50 ms / div.
Lower: \( I_{OUT} \), 1 A, 50 ms / div.
9.10  \textit{FWD Waveforms During Shorted Output}

\textbf{Figure 69} – FWD Voltage During Shorted Output. 
\[ V_{\text{IN}} = 400 \text{ VDC} \quad V_{\text{FWD(MAX)}} = 41 \text{ V}. \]
Upper: \( V_{\text{FWD}} \), 40 V, 500 ms / div.
Lower: Zoom @ 10 \( \mu \text{s} \) / div.

\textbf{Figure 70} – FWD Voltage During Shorted Output. 
\[ V_{\text{IN}} = 800 \text{ VDC} \quad V_{\text{FWD(MAX)}} = 79 \text{ V}. \]
Upper: \( V_{\text{FWD}} \), 40 V, 500 ms / div.
Lower: Zoom @ 10 \( \mu \text{s} \) / div.

\textbf{Figure 71} – FWD Voltage During Shorted Output. 
\[ V_{\text{IN}} = 1000 \text{ VDC} \quad V_{\text{FWD(MAX)}} = 98 \text{ V}. \]
Upper: \( V_{\text{FWD}} \), 40 V, 500 ms / div.
Lower: Zoom @ 10 \( \mu \text{s} \) / div.

\textbf{Figure 72} – FWD Voltage During Shorted Output. 
\[ V_{\text{IN}} = 1200 \text{ VDC} \quad V_{\text{FWD(MAX)}} = 119 \text{ V}. \]
Upper: \( V_{\text{FWD}} \), 40 V, 500 ms / div.
Lower: Zoom @ 10 \( \mu \text{s} \) / div.
10 Thermal Performance

All measurements have been done at room ambient temperature after 1 hour of continuous operation.

**Figure 73** – 400 VDC 1.25 A Full Load.
Temperature of INN3996CQ: 54.5 ºC.
Temperature of SR FET1(Q2): 54.3 ºC.
Temperature of SR FET2(Q3): 53.9 ºC.
Ambient Temperature: 28.5 ºC.

**Figure 74** – 800 VDC 1.25 A Full Load.
Temperature of INN3996CQ: 83.6 ºC.
Temperature of SR FET1(Q2): 61.2 ºC.
Temperature of SR FET2(Q3): 60.6 ºC.
Ambient Temperature: 29 ºC.

**Figure 75** – 1000 VDC 1.25 A Full Load.
Temperature of INN3996CQ: 97.8 ºC.
Temperature of SR FET1(Q2): 64.7 ºC.
Temperature of SR FET2(Q3): 64.0 ºC.
Ambient Temperature: 29.3 ºC.
10.1 *Temperature vs. Output Power*

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<th>SR FET (ºC)</th>
<th>TVS (ºC)</th>
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10.2 **Maximum Output Power vs. Ambient Temperature**  
(Based on 125 °C junction temperature of INN3996CQ)

![Graph showing Maximum Output Power vs. Ambient Temperature.](image)

**Figure 76** – Maximum Output Power vs. Ambient Temperature.
## 11 Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Author</th>
<th>Revision</th>
<th>Description &amp; Changes</th>
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<td>MA</td>
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<td>Change Minimum Input Voltage from 300 VDC to 40 VDC.</td>
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<td>10-Aug-21</td>
<td>KM</td>
<td>1.3</td>
<td>Fixed Typo in Section 2 and Updated the Format.</td>
<td>Mktg &amp; Apps</td>
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Power Integrations Worldwide Sales Support Locations

**WORLD HEADQUARTERS**
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

**CHINA (SHANGHAI)**
Rm 2410, Charity Plaza, No. 88, North Caoli Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasesales@power.com

**CHINA (SHENZHEN)**
17/F, Hivic Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasesales@power.com

**GERMANY (AC-DC/LED Sales)**
Einsteinring 24
85609 Domach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurorsales@power.com

**GERMANY (Gate Driver Sales)**
HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

**ITALY**
Via Milanese 20, 3rd Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurorsales@power.com

**JAPAN**
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

**KOREA**
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

**SINGAPORE**
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

**TAIWAN**
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2569-4570
e-mail: taiwansales@power.com

**UK**
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com