**Title**  
*Reference Design Report for a 30 W Power Supply Using InnoSwitch™3-AQ INN3977CQ*

<table>
<thead>
<tr>
<th>Specification</th>
<th>30 VDC – 550 VDC Input; 30 VDC – 12 V / 0.85 A; 60 VDC – 12 V / 1.25 A; 130-550 VDC – 12 V / 2.5 A Outputs</th>
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<tbody>
<tr>
<td>Application</td>
<td>Wide Input Range For Automotive</td>
</tr>
<tr>
<td>Author</td>
<td>Applications Engineering Department</td>
</tr>
<tr>
<td>Document Number</td>
<td>RDR-840Q</td>
</tr>
<tr>
<td>Date</td>
<td>April 6, 2021</td>
</tr>
<tr>
<td>Revision</td>
<td>1.4</td>
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**Summary and Features**

- Wide input voltage range: 30 VDC to 550 VDC
- InnoSwitch3-AQ – industry first AC/DC ICs with isolated, safety rated integrated feedback
- Built-in synchronous rectification for >85% efficiency
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing

**PATENT INFORMATION**

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.power.com](https://www.power.com). Power Integrations grants its customers a license under certain patent rights as set forth at [https://www.power.com/company/intellectual-property-licensing/](https://www.power.com/company/intellectual-property-licensing/).
Table of Contents

1 Introduction ...................................................................................................... 4
2 Power Supply Specification ................................................................................. 5
3 Schematic ......................................................................................................... 6
  3.1 SR FET Version .............................................................................................. 6
  3.2 Qspeed Diode Version .................................................................................. 7
4 Circuit Description .............................................................................................. 8
  4.1 INN3977CQ IC Primary .................................................................................. 8
  4.2 INN3977CQ IC Secondary .............................................................................. 8
5 PCB Layout ....................................................................................................... 9
6 Bill of Materials ................................................................................................ 11
  6.1 Main Board .................................................................................................... 11
  6.2 Mechanical Parts .......................................................................................... 12
7 Transformer Design ............................................................................................ 13
  7.1 Electrical Diagram ....................................................................................... 13
  7.2 Electrical Specifications ............................................................................... 13
  7.3 Material List .................................................................................................. 13
  7.4 Transformer Build Diagram ......................................................................... 14
  7.5 Transformer Instructions .............................................................................. 14
  7.6 Winding Illustrations .................................................................................... 15
8 Performance Data with SR FET version .............................................................. 21
  8.1 Average Efficiency ......................................................................................... 21
    8.1.1 30 VDC, 12 V 0.85 A (10 W) ................................................................ 21
    8.1.2 60 VDC, 12 V 1.25 A (15 W) ................................................................ 22
    8.1.3 130 VDC, 12 V 2.5 A (30 W) ................................................................ 23
    8.1.4 400 VDC, 12 V 2.5 A (30 W) ................................................................ 24
    8.1.5 550 VDC, 12 V 2.5 A (30 W) ................................................................ 25
  8.2 Efficiency vs. Load and Line ......................................................................... 26
    8.2.1 SR FET Version ..................................................................................... 26
    8.2.2 Qspeed Version ..................................................................................... 27
  8.3 No-Load Input Power .................................................................................... 28
  8.4 Load and Line Regulation ............................................................................ 29
  8.5 CV/CC ......................................................................................................... 30
9 Waveforms ....................................................................................................... 31
  9.1 Switching Waveforms .................................................................................. 31
    9.1.1 Drain Voltage and Current, Steady-State. ............................................ 31
    9.1.2 Drain Voltage and Current, Start-up. .................................................. 33
    9.1.3 SR FET Waveforms, Steady-State. ....................................................... 35
    9.1.4 SR FET Waveforms, Start-up. .............................................................. 37
    9.1.5 FWD Pin, Steady-State ......................................................................... 39
    9.1.6 FWD Pin, Start-up ................................................................................. 41
    9.1.7 Output Voltage and Current, Startup CR Load ...................................... 43
  9.2 Output Ripple Measurements (SR FET) ......................................................... 45
    9.2.1 Ripple Measurement Technique ............................................................ 45
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Page</th>
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<tbody>
<tr>
<td>9.2.2</td>
<td>100% Loading Condition</td>
<td>46</td>
</tr>
<tr>
<td>9.2.3</td>
<td>75% Loading Condition</td>
<td>48</td>
</tr>
<tr>
<td>9.2.4</td>
<td>50% Loading Condition</td>
<td>50</td>
</tr>
<tr>
<td>9.2.5</td>
<td>25% Loading Condition</td>
<td>52</td>
</tr>
<tr>
<td>9.2.6</td>
<td>0% Loading Condition</td>
<td>54</td>
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<tr>
<td>9.3</td>
<td><strong>Output Ripple Measurements (Qspeed Diode)</strong></td>
<td>56</td>
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<tr>
<td>9.3.1</td>
<td>100% Loading Condition</td>
<td>56</td>
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<tr>
<td>9.3.2</td>
<td>75% Loading Condition</td>
<td>57</td>
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<tr>
<td>9.3.3</td>
<td>50% Loading Condition</td>
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<tr>
<td>9.3.4</td>
<td>25% Loading Condition</td>
<td>59</td>
</tr>
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<td>9.3.5</td>
<td>0% Loading Condition</td>
<td>60</td>
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<td>9.4</td>
<td><strong>Output Load Transient</strong></td>
<td>61</td>
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<tr>
<td>9.4.1</td>
<td>Output Load Transient, 100% to 50% Load</td>
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<tr>
<td>9.4.2</td>
<td>Output Load Transient, 100% to 0% Load</td>
<td>63</td>
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<tr>
<td>9.5</td>
<td><strong>Output Short-Circuit Auto- Restart Test</strong></td>
<td>65</td>
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<td>10</td>
<td>Thermal Performance (SR FET)</td>
<td>67</td>
</tr>
<tr>
<td>10.1</td>
<td><strong>INN3977CQ Temperature Rise vs. Output Power</strong></td>
<td>69</td>
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<tr>
<td>12</td>
<td>Thermal Performance (Qspeed Diode)</td>
<td>70</td>
</tr>
<tr>
<td>13</td>
<td>-40 °C and +85 °C operational test</td>
<td>72</td>
</tr>
<tr>
<td>15</td>
<td>Revision History</td>
<td>73</td>
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</tbody>
</table>

**Important Note:**
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.
1 Introduction

This document is an engineering report describing a 30 VDC to 550 VDC input, 12 V output, 30 W Power Supply utilizing INN3977CQ from Power Integrations. The document contains the power supply specification, schematic, bill-of-materials and basic performance data.

Figure 1 – Populated Circuit Board Photograph, Top.

Figure 2 – Populated Circuit Board Photograph, Bottom.
### 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Comment</th>
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<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{IN}$</td>
<td>30</td>
<td>400</td>
<td>550</td>
<td>VDC</td>
<td>For Electric Vehicle Emergency PSU.</td>
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<tr>
<td>No-load Input Power (400VDC)</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>mW</td>
<td>@ 400 VDC.</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{OUT}$</td>
<td>12</td>
<td></td>
<td></td>
<td>V</td>
<td>±5%</td>
</tr>
<tr>
<td>Output Current</td>
<td>$I_{OUT}$</td>
<td>2.33</td>
<td></td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Output Ripple Voltage</td>
<td>$V_{RIPPLE}$</td>
<td>240</td>
<td></td>
<td></td>
<td>mV</td>
<td>On Board.</td>
</tr>
<tr>
<td><strong>Total Output Power</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous Output Power</td>
<td>$P_{OUT}$</td>
<td>30</td>
<td></td>
<td></td>
<td>W</td>
<td>$V_{IN}$ 130 VDC to 550 VDC.</td>
</tr>
<tr>
<td>Continuous Output Power</td>
<td>$P_{OUT}$</td>
<td>15</td>
<td></td>
<td></td>
<td>W</td>
<td>$V_{IN}$ of 60 VDC to 130 VDC.</td>
</tr>
<tr>
<td>Continuous Output Power</td>
<td>$P_{OUT}$</td>
<td>10</td>
<td></td>
<td></td>
<td>W</td>
<td>$V_{IN}$ of 30 VDC to 60 VDC.</td>
</tr>
<tr>
<td><strong>Isolation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Meets IEC 60664-1 as a minimum.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reinforce better</td>
</tr>
<tr>
<td><strong>Ambient Temperature</strong></td>
<td>$T_{AMB}$</td>
<td>-40</td>
<td></td>
<td>85</td>
<td>°C</td>
<td>Inside Inverter.</td>
</tr>
</tbody>
</table>
3  Schematic

3.1  **SR FET Version**

![Schematic with SR FET](image)

**Figure 3**  — Schematic with SR FET.
3.2 **Qspeed Diode Version**

![Schematic with Qspeed Diode](image)

**Figure 4** – Schematic with Qspeed Diode.
4 Circuit Description

4.1 INN3977CQ IC Primary
One end of the transformer primary is connected to the DC bus, the other is connected to the integrated power MOSFET inside the INN3977CQ IC (U1). High-voltage ceramic capacitor C1 is used for the decoupling capacitor for the DC input voltage, and a low cost RCD clamp formed by D2, R1, R2, R3, and C2 limits the peak Drain voltage due to the effects of transformer leakage inductance. Capacitor C15, Y capacitor, is used to attenuate the high frequency common mode noise on the output.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C4, when DC input voltage is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D3 and capacitor C3, and fed in the BPP pin via a current limiting resistor R4.

4.2 INN3977CQ IC Secondary
The secondary-side of the INN3977CQ IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 12 V output is provided by SR FETs Q1 and Q2. Low ESR capacitors, C7, C8, C9, C12, C13 and output inductor L1 provide filtering. Ceramic capacitor C15 attenuates high frequency noise on the output. RC snubber network comprising R7, R8 and C5 for Q1 and Q2 damps high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances. The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R5 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin. The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin. It will charge the decoupling capacitor C6 via an internal regulator.

Resistors R9 and R11 form a voltage divider network that senses the output voltage. INN3977CQ IC has an internal reference of 1.265 V. Capacitor C11 provides decoupling from high frequency noise affecting power supply operation, and C10 and R10 is the feedforward networks to speed up the response time to lower the output ripple. The output current is sensed by R6 with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold across these resistors is exceeded, the device adjusts the number of switch pulses to maintain a fixed output current.
5 PCB Layout

Figure 5 – Printed Circuit Board Layout (Top).

Figure 6 – Printed Circuit Board Layout (Bottom).
Figure 7 – Printed Circuit Board Layout (Internal layer 1).

Figure 8 – Printed Circuit Board Layout (Internal layer 2).
## 6 Bill of Materials

### 6.1 Main Board

<table>
<thead>
<tr>
<th>Item</th>
<th>Qty</th>
<th>Ref Des</th>
<th>Description</th>
<th>Mfg Part Number</th>
<th>Mfg</th>
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<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>C1</td>
<td>0.047 μF, ±10%, 1000 V (1kV), Ceramic, X7R, Automotive, AEC-Q200, 1812</td>
<td>1812Y1K00473KST</td>
<td>Knowles Syfer</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>C2</td>
<td>4700 pF, ±5%, 200V Ceramic COG, NP0 1206</td>
<td>CGJ5H3COG2D72J115AA</td>
<td>TDK</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>C3</td>
<td>22 μF, ±20%, 25 V, Ceramic, X5R, Automotive, AEC-Q200, 1206</td>
<td>1206D3226MAT2A</td>
<td>AVX</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>C4</td>
<td>0.47 μF, ±10%, 50 V, Ceramic, X7R, AEC-Q200, Automotive, 0805, -55°C ~ 125°C</td>
<td>CGA4J3X7R1H474K125AB</td>
<td>TDK</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>C5</td>
<td>2200 pF, ±10%, 200V, Ceramic, X7R, Automotive, AEC-Q200, 0805</td>
<td>08052C222K4T2A</td>
<td>AVX</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>C6</td>
<td>2.2 μF, 25 V, Ceramic, X7R, 0805</td>
<td>C2012X7R1E225M</td>
<td>TDK</td>
</tr>
<tr>
<td>7</td>
<td>3</td>
<td>C7 C8 C9</td>
<td>220 μF, 25 V, Electrolytic, Automotive, AEC-Q200, 0.260&quot; L x 0.260&quot; W (6.60 mm x 6.60 mm) x 0.315&quot; H (8.00 mm), SMD</td>
<td>EMZR250ARA21MF80G</td>
<td>United Chemicon</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>C10</td>
<td>10 nF, 50 V, Ceramic, X7R, Automotive, AEC-Q200, 0805</td>
<td>C0805C1035RACTU</td>
<td>Kemet</td>
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<tr>
<td>9</td>
<td>1</td>
<td>C11</td>
<td>330 pF, ±5%, 50V, Ceramic, COG, NP0, Automotive, AEC-Q200, 0603</td>
<td>C0603C331J5GAC</td>
<td>KEMET</td>
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<tr>
<td>10</td>
<td>1</td>
<td>C12</td>
<td>22 μF, 25 V, Ceramic, X7R, 1210</td>
<td>GRM32ER71E226KE15L</td>
<td>Murata</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>C13</td>
<td>100 μF, ±20%, 25 V, Z=320 mΩ, Electrolytic, Automotive, AEC-Q200, 0.260&quot; L x 0.260&quot; W (6.60 mm x 6.60 mm) x 0.315&quot; H (8.00 mm), SMD</td>
<td>UCD1E101MCL1GS</td>
<td>Nichicon</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>C14</td>
<td>1 μF, ±10%, 25V, X7R, 1206</td>
<td>C1206C105K3RAC</td>
<td>Kemet</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>C15</td>
<td>CAP, CER, 2200pF, ±20%, 760 VAC, Safety, Automotive, AEC-Q200, X1, Y1, Radial, Disc</td>
<td>AY1222M47Y5UC63L0</td>
<td>Vishay</td>
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<tr>
<td>14</td>
<td>1</td>
<td>D2</td>
<td>Diode, GEN PURP, 1000 V, 1 A, Automotive, AEC-Q101, DO214AC, DO-214AC (SMA)</td>
<td>US1MHE3_A/H</td>
<td>ON Semi</td>
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<tr>
<td>15</td>
<td>1</td>
<td>D3</td>
<td>Diode, General Purpose, 250 V,200 mA, Automotive, AEC-Q101, SC-76, SOD-323</td>
<td>NSVBA521AH1T1G</td>
<td>N/A</td>
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<td>16</td>
<td>2</td>
<td>FL1 FL2</td>
<td>Flying Lead, Hole size 70mils</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>17</td>
<td>1</td>
<td>L1</td>
<td>1.5 μH, ±20%, Shielded, Wirewound, Inductor, 4.5 A, 42 mΩ</td>
<td>SRP4020TA-1R5M</td>
<td>Bourns</td>
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<tr>
<td>18</td>
<td>2</td>
<td>Q1 Q2</td>
<td>MOSFET, N-Channel, 200 V, 13 A (Tc), 68 W (Tc), Automotive, AEC-Q101, PowerPAK® SO-8, PowerPAK SO-8</td>
<td>SQJ454EQP-T1_GE3</td>
<td>Vishay</td>
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<tr>
<td>19</td>
<td>1</td>
<td>R1</td>
<td>RES, 20 kΩ, 5%, 1/4 W, Automotive, AEC-Q200, Thick Film, 1206</td>
<td>ERJ-6GEY3203V</td>
<td>Panasonic</td>
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<tr>
<td>20</td>
<td>2</td>
<td>R2 R3</td>
<td>RES, 82 Ω, 5%, 1/4 W, Automotive, AEC-Q200, Thick Film, 1206</td>
<td>ERJ-6GEY3820V</td>
<td>Panasonic</td>
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<td>21</td>
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<td>R4</td>
<td>RES, 3.48 Ω, ±1%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805</td>
<td>ERJ-6ENF3481V</td>
<td>Panasonic</td>
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<td>22</td>
<td>1</td>
<td>R5</td>
<td>RES, SMD, 100 Ω, 1%, 1/10W, ±100ppm/°C, -55°C ~ 155°C, Moisture Resistant, Thick Film</td>
<td>RC0603FR-07100RL</td>
<td>Yageo</td>
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<tr>
<td>23</td>
<td>1</td>
<td>R6</td>
<td>0.011 Ω, ±1%, ±75ppm/°C, 1W, 1206, Automotive AEC-Q200, Current Sense, -55°C ~ 155°C</td>
<td>ERJ-8CWFR011V</td>
<td>Panasonic</td>
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<tr>
<td>24</td>
<td>2</td>
<td>R7 R8</td>
<td>RES, 20 Ω, 1%, 1/4 W, Automotive, AEC-Q200, Thick Film, 1206</td>
<td>ERJ-8ENF200R0V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>25</td>
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<td>R9</td>
<td>RES, 100 kΩ, 1%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805</td>
<td>ERJ-6ENF1003V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>26</td>
<td>1</td>
<td>R10</td>
<td>RES, 15 kΩ, 5%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805</td>
<td>ERJ-6GEY153V</td>
<td>Panasonic</td>
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<tr>
<td>27</td>
<td>1</td>
<td>R11</td>
<td>RES, 11.8 kΩ, 1%, 1/8 W, Automotive, AEC-Q200, Thick Film, 0805</td>
<td>ERJ-6ENF1182V</td>
<td>Panasonic</td>
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<tr>
<td>28</td>
<td>1</td>
<td>RD4</td>
<td>RES, 0 Ω, 5%, 1/4 W, Thick Film, 1206</td>
<td>ERJ-8GEYOR00V</td>
<td>Panasonic</td>
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<td>29</td>
<td>1</td>
<td>T1</td>
<td>Bobbin, EFD30, Horizontal, 12 pins Transformer</td>
<td>B66424-B1012-D1</td>
<td>Epcos Premier Magnetics</td>
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<tr>
<td>30</td>
<td>1</td>
<td>U1</td>
<td>InnoSwitch3-AQ InSOP24D</td>
<td>INN3977CQ</td>
<td>Power Integrations</td>
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### Mechanical Parts

<table>
<thead>
<tr>
<th>Item</th>
<th>Qty</th>
<th>Ref Des</th>
<th>Value</th>
<th>Description</th>
<th>Mfg Part Number</th>
<th>Mfg</th>
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<tbody>
<tr>
<td>31</td>
<td>2</td>
<td>RTN, VIN-</td>
<td>BLK</td>
<td>Test Point, BLK, THRU- HOLE MOUNT</td>
<td>5011</td>
<td>Keystone</td>
</tr>
<tr>
<td>32</td>
<td>2</td>
<td>VIN+, VO</td>
<td>RED</td>
<td>Test Point, RED, THRU- HOLE MOUNT</td>
<td>5010</td>
<td>Keystone</td>
</tr>
</tbody>
</table>
7 Transformer Design

7.1 Electrical Diagram

![Electrical Diagram](image)

**Figure 9 – Transformer Electrical Diagram.**

7.2 Electrical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Spec.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Primary Inductance</td>
<td>Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 3 and 6, with all other windings open.</td>
<td>950 μH ±5%</td>
</tr>
<tr>
<td>Resonant Frequency</td>
<td>Between pin 3 and 6, other windings open</td>
<td>1,100 kHz (Min.)</td>
</tr>
<tr>
<td>Primary Leakage Inductance</td>
<td>Between pin 3 and 6, with pins: FL1-FL2 shorted</td>
<td>4.5 μH (Max.)</td>
</tr>
</tbody>
</table>

7.3 Material List

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[8]</td>
<td>Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 20.4 mm Width.</td>
</tr>
<tr>
<td>[9]</td>
<td>Epoxy: Devcon, 5 mins Epoxy, Mfr#: 14270; or Equivalent.</td>
</tr>
</tbody>
</table>
7.4 **Transformer Build Diagram**

Figure 10 – Transformer Build Diagram.

7.5 **Transformer Instructions**

| Winding Preparation | Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side.  
|                     | Winding direction is clock-wise direction for forward direction. |
| WD1 1st Primary     | Start at pin 6, wind 27 bifilar turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 5.  
| Insulation          | 1 layer of tape Item [8]. |
| WD2: Bias & WD3: Shield | Use 2 wires Item [5] start at pin 1 for Bias winding, also use 2 wires same Item [5] start at pin 2 for Shield winding. Wind all 4 wires in parallel, at the 11th turn:  
|                     | - bring 2 wires for Bias winding to the left and terminate at pin 2,  
|                     | - cut short 2 wires for Shield Winding as No-Connect.  
| Insulation          | 1 layer of tape Item [8]. |
| WD4 Secondary       | Start at right slot of secondary side on the top of bobbin, use 3 wires Item [6], leaving ~50.0mm floating, and mark as FL1. Wind 10 turns in 1 layer, from right to left, at the last turn bring the wires back to the right, also leaving ~50.0mm floating, and mark FL2.  
| Insulation          | 1 layer of tape Item [8]. |
| WD5 2nd Primary     | Start at pin 5, wind 27 tri-filar turns of wire Item [4], from left to right for the 1st layer. Continue winding 3 more turns for the 2nd layer, spreading from right to left and terminate at pin 3.  
| Insulation          | 2 layers of tape Item [8] to secure the windings. |
| Finish              | Gap core halves to get 950 uH. Use 70mm of bus wire Item [7], solder to pin 2 then lean along core halves and secure with tape. Remove all secondary pins and cut short pin 5. Varnish with Item [11]. Place 2 beads of epoxy Item [9] at right and left, inside the cover Item [3]. Insert secondary side of the transformer into cover Item [3]. |
### 7.6 Winding Illustrations

#### Winding Preparation

Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clockwise direction for forward direction.

#### WD1 1st Primary

Start at pin 6, wind 27 bifilar turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and terminate at pin 5.
<table>
<thead>
<tr>
<th>Insulation</th>
<th>1 layer of tape Item [8].</th>
</tr>
</thead>
</table>
| **WD2: Bias** & **WD3: Shield** | Use 2 wires Item [5] start at pin 1 for Bias winding, also use 2 wires same Item [5] start at pin 2 for Shield winding. Wind all 4 wires in parallel, at the 11th turn:
- Bring 2 wires for Bias winding to the left and terminate at pin 2,
- Cut short 2 wires for Shield Winding as No-Connect. |
Insulation

1 layer of tape Item [8].

WD4 Secondary

Start at right slot of secondary side on the top of bobbin, use 3 wires Item [6], leaving ~ 50.0mm floating, and mark as FL1. Wind 10 turns in 1 layer, from right to left, at the last turn bring the wires back to the right, also leaving ~ 50.0mm floating, and mark FL2.
<table>
<thead>
<tr>
<th>Insulation</th>
<th></th>
<th>1 layer of tape Item [8].</th>
</tr>
</thead>
<tbody>
<tr>
<td>WD5</td>
<td>FL1</td>
<td>Start at pin 5, wind 27 trifilar turns of wire Item [4], from left to right for the 1st layer. Continue winding 3 more turns for the 2nd layer, spreading from right to left and terminate at pin 3.</td>
</tr>
<tr>
<td>2nd Primary</td>
<td>FL2</td>
<td></td>
</tr>
</tbody>
</table>
Insulation

2 layers of tape Item [8] to secure the windings.

Finish

Gap core halves to get 950uH. Use 70mm of bus wire Item [7], solder to pin 2 then lean along core halves and secure with tape. Remove all secondary pins and cut short pin 5. Varnish with Item [11]. Place 2 beads of epoxy Item [9] at right and left, inside the cover Item [3].
Insert secondary side of the transformer into cover Item [3].
8  Performance Data with SR FET version
All measurements performed with room ambient temperature. Measured at PCB output terminal.

8.1  Average Efficiency

8.1.1  30 VDC, 12 V 0.85 A (10 W)

8.1.1.1  SR FET Version

<table>
<thead>
<tr>
<th>Load (%)</th>
<th>V_OUT (V)</th>
<th>I_OUT (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>11.50</td>
<td>848.56</td>
<td>87.71</td>
</tr>
<tr>
<td>75%</td>
<td>11.60</td>
<td>636.59</td>
<td>87.93</td>
</tr>
<tr>
<td>50%</td>
<td>11.70</td>
<td>424.63</td>
<td>87.12</td>
</tr>
<tr>
<td>25%</td>
<td>11.84</td>
<td>212.31</td>
<td>84.49</td>
</tr>
<tr>
<td>10%</td>
<td>11.92</td>
<td>85.06</td>
<td>76.28</td>
</tr>
<tr>
<td>Average</td>
<td></td>
<td></td>
<td><strong>86.69</strong></td>
</tr>
</tbody>
</table>

8.1.1.2  Qspeed Version

<table>
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<th>V_OUT (V)</th>
<th>I_OUT (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>11.58</td>
<td>849.25</td>
<td>83.71</td>
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<tr>
<td>75%</td>
<td>11.68</td>
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<td>83.96</td>
</tr>
<tr>
<td>50%</td>
<td>11.78</td>
<td>423.25</td>
<td>82.97</td>
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<tr>
<td>25%</td>
<td>11.91</td>
<td>209.63</td>
<td>79.90</td>
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<tr>
<td>10%</td>
<td>11.99</td>
<td>82.13</td>
<td>71.46</td>
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<tr>
<td>Average</td>
<td></td>
<td></td>
<td><strong>82.64</strong></td>
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</tbody>
</table>
8.1.2 60 VDC, 12 V 1.25 A (15 W)

8.1.2.1 SR FET Version

<table>
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<tr>
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<th>V_out (V)</th>
<th>I_out (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>1241.88</td>
<td>89.97</td>
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<tr>
<td>75%</td>
<td>11.81</td>
<td>929.38</td>
<td>90.48</td>
</tr>
<tr>
<td>50%</td>
<td>11.98</td>
<td>619.06</td>
<td>89.33</td>
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<tr>
<td>25%</td>
<td>11.96</td>
<td>305.94</td>
<td>87.86</td>
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<tr>
<td>10%</td>
<td>11.93</td>
<td>120.00</td>
<td>79.64</td>
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</table>

Average 89.40

8.1.2.2 Qspeed Version

<table>
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<th>I_out (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>11.84</td>
<td>1250.25</td>
<td>85.65</td>
</tr>
<tr>
<td>75%</td>
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<td>85.66</td>
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<tr>
<td>50%</td>
<td>12.01</td>
<td>623.88</td>
<td>84.86</td>
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<td>25%</td>
<td>12.01</td>
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<tr>
<td>10%</td>
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<td>122.13</td>
<td>76.00</td>
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</table>

Average 84.88
8.1.3 130 VDC, 12 V 2.5 A (30 W)

8.1.3.1 SR FET Version

<table>
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<tr>
<th>Load</th>
<th>V_{OUT} (V)</th>
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<th>Efficiency (%)</th>
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<td>88.56</td>
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<tr>
<td>10%</td>
<td>11.95</td>
<td>250.00</td>
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8.1.3.2 Qspeed Version

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<td>11.94</td>
<td>1877.50</td>
<td>86.41</td>
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<td>50%</td>
<td>12.05</td>
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<td>12.04</td>
<td>623.88</td>
<td>84.63</td>
</tr>
<tr>
<td>10%</td>
<td>12.01</td>
<td>247.38</td>
<td>80.06</td>
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<tr>
<td></td>
<td><strong>Average</strong></td>
<td></td>
<td><strong>86.07</strong></td>
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</tbody>
</table>
8.1.4  400 VDC, 12 V 2.5 A (30 W)

8.1.4.1  SR FET Version

<table>
<thead>
<tr>
<th>Load</th>
<th>V_{\text{out}} (V)</th>
<th>I_{\text{out}} (mA)</th>
<th>Efficiency (%)</th>
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</thead>
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<td>87.38</td>
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<td>1873.44</td>
<td>87.73</td>
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<tr>
<td>50%</td>
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<td>25%</td>
<td>12.02</td>
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<td>83.36</td>
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<tr>
<td>10%</td>
<td>11.96</td>
<td>250.00</td>
<td>78.25</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Average 86.40</strong></td>
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8.1.4.2  Qspeed Version

<table>
<thead>
<tr>
<th>Load</th>
<th>V_{\text{out}} (V)</th>
<th>I_{\text{out}} (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>11.99</td>
<td>2504.25</td>
<td>87.69</td>
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<tr>
<td>75%</td>
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<tr>
<td>50%</td>
<td>12.08</td>
<td>1250.25</td>
<td>83.73</td>
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<tr>
<td>25%</td>
<td>12.07</td>
<td>623.88</td>
<td>80.25</td>
</tr>
<tr>
<td>10%</td>
<td>12.01</td>
<td>247.38</td>
<td>73.92</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Average 83.89</strong></td>
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</tbody>
</table>
8.1.5  550 VDC, 12 V 2.5 A (30 W)

8.1.5.1  SR FET Version

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<th>Load</th>
<th>V\textsubscript{OUT} (V)</th>
<th>I\textsubscript{OUT} (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>1877.50</td>
<td>84.98</td>
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<tr>
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<td>12.08</td>
<td>1250.38</td>
<td>83.51</td>
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<td>12.04</td>
<td>623.75</td>
<td>79.15</td>
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<td>10%</td>
<td>11.99</td>
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<td>72.54</td>
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<td>Average</td>
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<td><strong>83.49</strong></td>
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8.1.5.2  Qspeed Version

<table>
<thead>
<tr>
<th>Load</th>
<th>V\textsubscript{OUT} (V)</th>
<th>I\textsubscript{OUT} (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>11.94</td>
<td>2504.25</td>
<td>81.99</td>
</tr>
<tr>
<td>75%</td>
<td>12.09</td>
<td>1877.63</td>
<td>83.83</td>
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<tr>
<td>50%</td>
<td>12.09</td>
<td>1250.25</td>
<td>81.33</td>
</tr>
<tr>
<td>25%</td>
<td>12.06</td>
<td>623.75</td>
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<td>10%</td>
<td>12.02</td>
<td>247.38</td>
<td>69.62</td>
</tr>
<tr>
<td>Average</td>
<td></td>
<td></td>
<td><strong>81.30</strong></td>
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</tbody>
</table>
8.2 Efficiency vs. Load and Line

Measurements taken at 0% to 100% of rated load.

8.2.1 SR FET Version

![Efficiency vs. Load and Line (VDC), Room Temperature – SR FET Version.](image)

**Figure 11** – Efficiency vs. Load and Line (VDC), Room Temperature – SR FET Version.
8.2.2 Qspeed Version

Figure 12 – Efficiency vs. Load and Line (VDC), Room Temperature – Qspeed Version.
8.3 **No-Load Input Power**

![Graph showing No-Load Input Power](image)

*Figure 13 – No-Load Input Power, Room Temperature.*
8.4 **Load and Line Regulation**

Measurements taken at 0% to 100% of rated load.

![Graph showing output voltage vs. output current and input voltage (VDC), room temperature.](image)

**Figure 14** – Output Voltage vs. Output Current and Input Voltage (VDC), Room Temperature.
8.5 **CV/CC**

![CV/CC graph](image)

**Figure 15** – CV/CC measured at PCB Output Terminal, Room Temperature.

---

Power Integrations, Inc.
Tel: +1 408 414 9200   Fax: +1 408 414 9201
www.power.com
9  Waveforms

9.1  Switching Waveforms

9.1.1  Drain Voltage and Current, Steady-State.

**Figure 16** – Drain Voltage and Current Waveforms.  
$V_{IN} = 30 \text{ VDC}, I_{OUT} = 0.85 \text{ A}$.  
$V_{DS(MAX)} = 149 \text{ V}, I_{DRAIN(MAX)} = 1.41 \text{ A}$.  
Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.  
Lower: $I_{DRAIN}$, 500 mA, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 17** – Drain Voltage and Current Waveforms.  
$V_{IN} = 60 \text{ VDC}, I_{OUT} = 1.25 \text{ A}$.  
$V_{DS(MAX)} = 185 \text{ V}, I_{DRAIN(MAX)} = 1.16 \text{ A}$.  
Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.  
Lower: $I_{DRAIN}$, 500 mA, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 18** – Drain Voltage and Current Waveforms.  
$V_{IN} = 130 \text{ VDC}, I_{OUT} = 2.5 \text{ A}$.  
$V_{DS(MAX)} = 262 \text{ V}, I_{DRAIN(MAX)} = 2.14 \text{ A}$.  
Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.  
Lower: $I_{DRAIN}$, 500 mA, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 19** – Drain Voltage and Current Waveforms.  
$V_{IN} = 400 \text{ VDC}, I_{OUT} = 2.5 \text{ A}$.  
$V_{DS(MAX)} = 548 \text{ V}, I_{DRAIN(MAX)} = 1.64 \text{ A}$.  
Upper: $V_{DRAIN-SOURCE}$, 200 V, 2 ms / div.  
Lower: $I_{DRAIN}$, 500 mA, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.
Figure 20 – Drain Voltage and Current Waveforms. 
\( V_{IN} = 550 \text{ VDC}, \ I_{OUT} = 2.5 \text{ A}. \) 
\( V_{DS(\text{MAX})} = 693 \text{ V}, \ I_{\text{DRAIN(\text{MAX})}} = 2.14 \text{ A}. \) 
Upper: \( V_{\text{DRAIN-SOURCE}}, 200 \text{ V}, 2 \text{ ms / div}. \) 
Lower: \( I_{\text{DRAIN}}, 500 \text{ mA}, 2 \text{ ms / div}. \) 
Bottom Half: Zoom @ 10 \( \mu \text{s / div}. \)
9.1.2 Drain Voltage and Current, Start-up.

**Figure 21** – Drain Voltage and Current Waveforms.
\[ V_{IN} = 30 \text{ VDC}, \; I_{OUT} = 0.85 \text{ A}. \]
\[ V_{DS(\text{MAX})} = 154 \text{ V}, \; I_{\text{DRAIN(\text{MAX})}} = 2.38 \text{ A}. \]
Upper: \( V_{\text{DRAIN-SOURCE}} \), 200 V, 50 ms / div.
Lower: \( I_{\text{DRAIN}} \), 1 A, 50 ms / div.

**Figure 22** – Drain Voltage and Current Waveforms.
\[ V_{IN} = 60 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A}. \]
\[ V_{DS(\text{MAX})} = 191 \text{ V}, \; I_{\text{DRAIN(\text{MAX})}} = 2.17 \text{ A}. \]
Upper: \( V_{\text{DRAIN-SOURCE}} \), 200 V, 50 ms / div.
Lower: \( I_{\text{DRAIN}} \), 1 A, 50 ms / div.

**Figure 23** – Drain Voltage and Current Waveforms.
\[ V_{IN} = 130 \text{ VDC}, \; I_{OUT} = 2.5 \text{ A}. \]
\[ V_{DS(\text{MAX})} = 266 \text{ V}, \; I_{\text{DRAIN(\text{MAX})}} = 2.80 \text{ A}. \]
Upper: \( V_{\text{DRAIN-SOURCE}} \), 200 V, 50 ms / div.
Lower: \( I_{\text{DRAIN}} \), 1 A, 50 ms / div.

**Figure 24** – Drain Voltage and Current Waveforms.
\[ V_{IN} = 400 \text{ VDC}, \; I_{OUT} = 2.5 \text{ A}. \]
\[ V_{DS(\text{MAX})} = 541 \text{ V}, \; I_{\text{DRAIN(\text{MAX})}} = 4.03 \text{ A}. \]
Upper: \( V_{\text{DRAIN-SOURCE}} \), 200 V, 50 ms / div.
Lower: \( I_{\text{DRAIN}} \), 1 A, 50 ms / div.
**Figure 25** – Drain Voltage and Current Waveforms.  
$V_{IN} = 550$ VDC, $I_{OUT} = 2.5$ A.  
$V_{DS(MAX)} = 692$ V, $I_{DRAIN(MAX)} = 4.03$ A.  
*Upper:* $V_{DRAIN-SOURCE}$, 200 V, 50 ms / div.  
*Lower:* $I_{DRAIN}$, 1 A, 50 ms / div.
9.1.3 SR FET Waveforms, Steady-State.

**Figure 26** – Drain Voltage and Current Waveforms.  
$V_{IN} = 30$ VDC, $I_{OUT} = 0.85$ A.  
$V_{DS(MAX)} = 41$ V, $I_{DRAIN(MAX)} = 6.0$ A.  
**Upper:** $I_{DRAIN}$, 5 A, 2 ms / div.  
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div.  
**Lower:** $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 27** – Drain Voltage and Current Waveforms.  
$V_{IN} = 60$ VDC, $I_{OUT} = 1.25$ A.  
$V_{DS(MAX)} = 44$ V, $I_{DRAIN(MAX)} = 5.0$ A.  
**Upper:** $I_{DRAIN}$, 5 A, 2 ms / div.  
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div.  
**Lower:** $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 28** – Drain Voltage and Current Waveforms.  
$V_{IN} = 130$ VDC, $I_{OUT} = 2.5$ A.  
$V_{DS(MAX)} = 73$ V, $I_{DRAIN(MAX)} = 7.7$ A.  
**Upper:** $I_{DRAIN}$, 5 A, 2 ms / div.  
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div.  
**Lower:** $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.

**Figure 29** – Drain Voltage and Current Waveforms.  
$V_{IN} = 400$ VDC, $I_{OUT} = 2.5$ A.  
$V_{DS(MAX)} = 101$ V, $I_{DRAIN(MAX)} = 1.37$ A.  
**Upper:** $I_{DRAIN}$, 5 A, 2 ms / div.  
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div.  
**Lower:** $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div.  
Bottom Half: Zoom @ 10 $\mu$s / div.
Figure 30 – Drain Voltage and Current Waveforms.

- **V\textsubscript{IN} = 550 VDC, I\textsubscript{OUT} = 2.5 A.**
- **V\textsubscript{DS(MAX)} = 131 V, I\textsubscript{DRAIN(MAX)} = 8.0 A.**
- **Upper:** I\textsubscript{DRAIN}, 5 A, 2 ms / div.
- **Middle:** V\textsubscript{GATE-SOURCE}, 5 V, 2 ms / div.
- **Lower:** V\textsubscript{DRAIN-SOURCE}, 50 V, 2 ms / div.
- **Bottom Half:** Zoom @ 10 μs / div.
9.1.4 SR FET Waveforms, Start-up.

**Figure 31** – Drain Voltage and Current Waveforms. 
$V_{IN} = 30 \text{ VDC}, I_{OUT} = 0.85 \text{ A}$. 
$V_{DS(\text{MAX})} = 48.4 \text{ V}, I_{DRAIN(\text{MAX})} = 0.851 \text{ A}$. 
**Upper:** $I_{DRAIN}$, 10 A, 2 ms / div. 
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div. 
**Lower:** $V_{DRAIN-SOURCE}$, 20 V, 2 ms / div. 
Bottom Half: Zoom @ 50 μs / div.

**Figure 32** – Drain Voltage and Current Waveforms. 
$V_{IN} = 60 \text{ VDC}, I_{OUT} = 1.25 \text{ A}$. 
$V_{DS(\text{MAX})} = 57.8 \text{ V}, I_{DRAIN(\text{MAX})} = 1.57 \text{ A}$. 
**Upper:** $I_{DRAIN}$, 10 A, 2 ms / div. 
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div. 
**Lower:** $V_{DRAIN-SOURCE}$, 20 V, 2 ms / div. 
Bottom Half: Zoom @ 50 μs / div.

**Figure 33** – Drain Voltage and Current Waveforms. 
$V_{IN} = 130 \text{ VDC}, I_{OUT} = 2.5 \text{ A}$. 
$V_{DS(\text{MAX})} = 86 \text{ V}, I_{DRAIN(\text{MAX})} = 8.0 \text{ A}$. 
**Upper:** $I_{DRAIN}$, 5 A, 2 ms / div. 
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div. 
**Lower:** $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div. 
Bottom Half: Zoom @ 50 μs / div.

**Figure 34** – Drain Voltage and Current Waveforms. 
$V_{IN} = 400 \text{ VDC}, I_{OUT} = 2.5 \text{ A}$. 
$V_{DS(\text{MAX})} = 145 \text{ V}, I_{DRAIN(\text{MAX})} = 7.7 \text{ A}$. 
**Upper:** $I_{DRAIN}$, 5 A, 2 ms / div. 
**Middle:** $V_{GATE-SOURCE}$, 5 V, 2 ms / div. 
**Lower:** $V_{DRAIN-SOURCE}$, 50 V, 2 ms / div. 
Bottom Half: Zoom @ 50 μs / div.
Figure 35 – Drain Voltage and Current Waveforms.

\[ V_{\text{IN}} = 550 \text{ VDC}, \quad I_{\text{OUT}} = 2.5 \text{ A}. \]

\[ V_{\text{DS(MAX)}} = 149 \text{ V}, \quad I_{\text{DRAIN(MAX)}} = 8.0 \text{ A}. \]

**Upper:** \( I_{\text{DRAIN}}, 10 \text{ A}, 2 \text{ ms / div.} \)

**Middle:** \( V_{\text{GATE-SOURCE}}, 5 \text{ V}, 2 \text{ ms / div.} \)

**Lower:** \( V_{\text{DRAIN-SOURCE}}, 50 \text{ V}, 2 \text{ ms / div.} \)

**Bottom Half:** Zoom @ 50 \( \mu \text{s / div.} \)
9.1.5 FWD Pin, Steady-State

**Figure 36** – Drain Voltage and Current Waveforms. $V_{IN} = 30 \text{ VDC}, I_{OUT} = 0.85 \text{ A}$. $V_{FWD(MAX)} = 39.6 \text{ V}$

Upper: $V_{FWD}$, 20 V, 50 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.

**Figure 37** – Drain Voltage and Current Waveforms. $V_{IN} = 60 \text{ VDC}, I_{OUT} = 1.25 \text{ A}$. $V_{FWD(MAX)} = 34.6 \text{ V}$

Upper: $V_{FWD}$, 20 V, 50 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.

**Figure 38** – Drain Voltage and Current Waveforms. $V_{IN} = 130 \text{ VDC}, I_{OUT} = 2.5 \text{ A}$. $V_{FWD(MAX)} = 66.0 \text{ V}$

Upper: $V_{FWD}$, 20 V, 50 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.

**Figure 39** – Drain Voltage and Current Waveforms. $V_{IN} = 400 \text{ VDC}, I_{OUT} = 2.5 \text{ A}$. $V_{FWD(MAX)} = 98.0 \text{ V}$

Upper: $V_{FWD}$, 20 V, 50 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.
Figure 40 — Drain Voltage and Current Waveforms. 
\( V_{\text{IN}} = 550 \, \text{VDC}, \, I_{\text{OUT}} = 2.5 \, \text{A} \).  
\( V_{\text{FWD(MAX)}} = 126.8 \, \text{V} \) 
**Upper:** \( V_{\text{FWD}} \), 20 V, 50 ms / div. 
**Bottom Half:** Zoom @ 20 \( \mu \text{s} / \text{div} \).
9.1.6 FWD Pin, Start-up

**Figure 41** – Drain Voltage and Current Waveforms.
- \( V_{IN} = 30 \, VDC \), \( I_{OUT} = 0.85 \, A \).
- \( V_{FWD(MAX)} = 43.4 \, V \)
  - **Upper**: \( V_{FWD} \), 20 V, 50 ms / div.
  - **Bottom Half**: Zoom @ 20 \( \mu \)s / div.

**Figure 42** – Drain Voltage and Current Waveforms.
- \( V_{IN} = 60 \, VDC \), \( I_{OUT} = 1.25 \, A \).
- \( V_{FWD(MAX)} = 52.6 \, V \)
  - **Upper**: \( V_{FWD} \), 20 V, 50 ms / div.
  - **Bottom Half**: Zoom @ 20 \( \mu \)s / div.

**Figure 43** – Drain Voltage and Current Waveforms.
- \( V_{IN} = 130 \, VDC \), \( I_{OUT} = 2.5 \, A \).
- \( V_{FWD(MAX)} = 79.6 \, V \)
  - **Upper**: \( V_{FWD} \), 20 V, 50 ms / div.
  - **Bottom Half**: Zoom @ 20 \( \mu \)s / div.

**Figure 44** – Drain Voltage and Current Waveforms.
- \( V_{IN} = 400 \, VDC \), \( I_{OUT} = 2.5 \, A \).
- \( V_{FWD(MAX)} = 115.2 \, V \)
  - **Upper**: \( V_{FWD} \), 20 V, 50 ms / div.
  - **Bottom Half**: Zoom @ 20 \( \mu \)s / div.
**Figure 45** – Drain Voltage and Current Waveforms.

- $V_{\text{IN}} = 550$ VDC, $I_{\text{OUT}} = 2.5$ A.
- $V_{\text{FWD}(\text{MAX})} = 127.5$ V
  - **Upper:** $V_{\text{FWD}}$, 20 V, 50 ms / div.
  - **Bottom Half:** Zoom @ 20 $\mu$s / div.
9.1.7 Output Voltage and Current, Startup CR Load

**Figure 46** – Drain Voltage and Current Waveforms. 
\(V_{\text{IN}} = 30 \text{ VDC}, I_{\text{OUT}} = 0.85 \text{ A CR Load.}
\)
Upper: \(V_{\text{OUT}},\) 5 V, 20 ms / div.
Lower: \(I_{\text{DRAIN}},\) 1 A, 20 ms / div.

**Figure 47** – Drain Voltage and Current Waveforms. 
\(V_{\text{IN}} = 60 \text{ VDC}, I_{\text{OUT}} = 1.25 \text{ A CR Load.}
\)
Upper: \(V_{\text{OUT}},\) 5 V, 20 ms / div.
Lower: \(I_{\text{DRAIN}},\) 1 A, 20 ms / div.

**Figure 48** – Drain Voltage and Current Waveforms. 
\(V_{\text{IN}} = 130 \text{ VDC}, I_{\text{OUT}} = 2.5 \text{ A CR Load.}
\)
Upper: \(V_{\text{OUT}},\) 5 V, 20 ms / div.
Lower: \(I_{\text{DRAIN}},\) 1 A, 20 ms / div.

**Figure 49** – Drain Voltage and Current Waveforms. 
\(V_{\text{IN}} = 400 \text{ VDC}, I_{\text{OUT}} = 2.5 \text{ A CR Load.}
\)
Upper: \(V_{\text{OUT}},\) 5 V, 20 ms / div.
Lower: \(I_{\text{DRAIN}},\) 1 A, 20 ms / div.
**Figure 50** — Drain Voltage and Current Waveforms.

$V_{IN} = 550$ VDC, $I_{OUT} = 2.5$ A CR Load.

Upper: $V_{OUT}$, 5 V, 20 ms / div.
Lower: $I_{DRAIN}$, 1 A, 20 ms / div.
9.2 **Output Ripple Measurements (SR FET)**

9.2.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor include one (1) $1 \mu F/50$ V ceramic type.

![Figure 51](image1.png)  
**Figure 51** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

![Figure 52](image2.png)  
**Figure 52** – Oscilloscope Probe with Probe Master ([www.probemaster.com](http://www.probemaster.com)) 4987A BNC Adapter. (Modified with wires for ripple measurement, and one parallel decoupling capacitor added)
9.2.2 100% Loading Condition

Figure 53 – Output Voltage Ripple.
\( V_{\text{IN}} = 30 \text{ VDC}, I_{\text{OUT}} = 0.85 \text{ A} \).
Top Half: \( V_{\text{OUT}}, 50 \text{ mV}, 5 \text{ ms / div.} \)
Bottom Half: Zoom @ 20 \( \mu \text{s / div.} \)
\( V_{\text{RIPPLE}} = 104 \text{ mV}_{\text{P-P}} \)

Figure 54 – Output Voltage Ripple.
\( V_{\text{IN}} = 60 \text{ VDC}, I_{\text{OUT}} = 1.25 \text{ A} \).
Top Half: \( V_{\text{OUT}}, 50 \text{ mV}, 5 \text{ ms / div.} \)
Bottom Half: Zoom @ 20 \( \mu \text{s / div.} \)
\( V_{\text{RIPPLE}} = 133 \text{ mV}_{\text{P-P}} \)

Figure 55 – Output Voltage Ripple.
\( V_{\text{IN}} = 130 \text{ VDC}, I_{\text{OUT}} = 2.5 \text{ A} \).
Top Half: \( V_{\text{OUT}}, 50 \text{ mV}, 5 \text{ ms / div.} \)
Bottom Half: Zoom @ 20 \( \mu \text{s / div.} \)
\( V_{\text{RIPPLE}} = 107 \text{ mV}_{\text{P-P}} \)

Figure 56 – Output Voltage Ripple.
\( V_{\text{IN}} = 400 \text{ VDC}, I_{\text{OUT}} = 2.5 \text{ A} \).
Top Half: \( V_{\text{OUT}}, 50 \text{ mV}, 5 \text{ ms / div.} \)
Bottom Half: Zoom @ 20 \( \mu \text{s / div.} \)
\( V_{\text{RIPPLE}} = 170 \text{ mV}_{\text{P-P}} \)
Figure 57 – Output Voltage Ripple.

$V_{IN} = 550$ VDC, $I_{OUT} = 2.5$ A.
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.
$V_{RIPPLE} = 170$ mVp-p
9.2.3 75% Loading Condition

**Figure 58** – Output Voltage Ripple. 
VIN = 30 VDC, IOUT = 0.85 A.  
Top Half: VOUT, 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 20 μs / div.  
V<sub>RIPPLE</sub> = 85 mV<sub>p-p</sub>

**Figure 59** – Output Voltage Ripple.  
VIN = 60 VDC, IOUT = 1.25 A.  
Top Half: VOUT, 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 20 μs / div.  
V<sub>RIPPLE</sub> = 160 mV<sub>p-p</sub>

**Figure 60** – Output Voltage Ripple.  
VIN = 130 VDC, IOUT = 2.5 A.  
Top Half: VOUT, 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 20 μs / div.  
V<sub>RIPPLE</sub> = 123 mV<sub>p-p</sub>

**Figure 61** – Output Voltage Ripple.  
VIN = 400 VDC, IOUT = 2.5 A.  
Top Half: VOUT, 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 20 μs / div.  
V<sub>RIPPLE</sub> = 178 mV<sub>p-p</sub>
Figure 62 — Output Voltage Ripple.

$\text{VIN} = 550 \, \text{VDC}, \, \text{IOUT} = 2.5 \, \text{A}.$

Top Half: $V_{\text{OUT}}$, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.

$V_{\text{RIPPLE}} = 178 \, \text{mV}_{\text{P-P}}$
9.2.4 50% Loading Condition

Figure 63 – Output Voltage Ripple. $V_{IN} = 30$ VDC, $I_{OUT} = 0.85$ A.
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.
$V_{RIPPLE} = 70$ mVP-P

Figure 64 – Output Voltage Ripple. $V_{IN} = 60$ VDC, $I_{OUT} = 1.25$ A.
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.
$V_{RIPPLE} = 133$ mVP-P

Figure 65 – Output Voltage Ripple. $V_{IN} = 130$ VDC, $I_{OUT} = 2.5$ A.
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.
$V_{RIPPLE} = 138$ mVP-P

Figure 66 – Output Voltage Ripple. $V_{IN} = 400$ VDC, $I_{OUT} = 2.5$ A.
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.
$V_{RIPPLE} = 162$ mVP-P
Figure 67 – Output Voltage Ripple.

$V_{IN} = 550$ VDC, $I_{OUT} = 2.5$ A.
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 $\mu$s / div.
$V_{RIPPLE} = 163$ mV-P-P
9.2.5 25% Loading Condition

Figure 68 – Output Voltage Ripple.
VIN = 30 VDC, IOUT = 0.85 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 192 mVP-P

Figure 69 – Output Voltage Ripple.
VIN = 60 VDC, IOUT = 1.25 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 99 mVP-P

Figure 70 – Output Voltage Ripple.
VIN = 130 VDC, IOUT = 2.5 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 104 mVP-P

Figure 71 – Output Voltage Ripple.
VIN = 400 VDC, IOUT = 2.5 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 82 mVP-P
Figure 72 – Output Voltage Ripple.

\[ V_{IN} = 550 \text{ VDC}, \; I_{OUT} = 2.5 \text{ A}. \]

Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.

Bottom Half: Zoom @ 20 \( \mu \text{s} \) / div.

\[ V_{RIPIPE} = 128 \text{ mV}_{P-P} \]
9.2.6 0% Loading Condition

Figure 73 – Output Voltage Ripple.
VIN = 30 VDC, IOUT = 0.85 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 37 mVP-P

Figure 74 – Output Voltage Ripple.
VIN = 60 VDC, IOUT = 1.25 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 45 mVP-P

Figure 75 – Output Voltage Ripple.
VIN = 130 VDC, IOUT = 2.5 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 32 mVP-P

Figure 76 – Output Voltage Ripple.
VIN = 400 VDC, IOUT = 2.5 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 μs / div.
VRIPPLE = 54 mVP-P
Figure 77 – Output Voltage Ripple.  
\[ V_{IN} = 550 \text{ VDC}, \quad I_{OUT} = 2.5 \text{ A}. \]  
Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 20 \( \mu \text{s} \) / div.  
\[ V_{RIPPLE} = 53 \text{ mV}_{\text{P-P}} \]
9.3 **Output Ripple Measurements (Qspeed Diode)**

9.3.1 **100% Loading Condition**

*Figure 78 – Output Voltage Ripple.*

\[ V_{IN} = 130 \text{ VDC}, \ I_{OUT} = 2.5 \text{ A}. \]

Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 \( \mu \text{s} / \text{div}. \)

\[ V_{RIPPLE} = 112 \text{ mVP-P} \]

*Figure 79 – Output Voltage Ripple.*

\[ V_{IN} = 400 \text{ VDC}, \ I_{OUT} = 2.5 \text{ A}. \]

Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 \( \mu \text{s} / \text{div}. \)

\[ V_{RIPPLE} = 146 \text{ mVP-P} \]

*Figure 80 – Output Voltage Ripple.*

\[ V_{IN} = 550 \text{ VDC}, \ I_{OUT} = 2.5 \text{ A}. \]

Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 \( \mu \text{s} / \text{div}. \)

\[ V_{RIPPLE} = 170 \text{ mVP-P} \]
9.3.2 75% Loading Condition

**Figure 81** – Output Voltage Ripple.
VIN = 130 VDC, IOUT = 1.875 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 μs / div.
VRIPPLE = 109 mVp-p

**Figure 82** – Output Voltage Ripple.
VIN = 400 VDC, IOUT = 1.875 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 μs / div.
VRIPPLE = 155 mVp-p

**Figure 83** – Output Voltage Ripple.
VIN = 550 VDC, IOUT = 1.875 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 μs / div.
VRIPPLE = 187 mVp-p
9.3.3 50% Loading Condition

Figure 84 – Output Voltage Ripple.
\[ V_{IN} = 130 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A} \]
Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 \( \mu \text{s} \) / div.
VRIPPLE = 120 mVP-P

Figure 85 – Output Voltage Ripple.
\[ V_{IN} = 400 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A} \]
Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 \( \mu \text{s} \) / div.
VRIPPLE = 165 mVP-P

Figure 86 – Output Voltage Ripple.
\[ V_{IN} = 550 \text{ VDC}, \; I_{OUT} = 1.25 \text{ A} \]
Top Half: \( V_{OUT} \), 50 mV, 5 ms / div.
Bottom Half: Zoom @ 20 \( \mu \text{s} \) / div.
VRIPPLE = 184 mVP-P
9.3.4 25% Loading Condition

**Figure 87** – Output Voltage Ripple.  
$V_{IN} = 130$ VDC, $I_{OUT} = 0.625$ A.  
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 50 $\mu$s / div.  
$V_{RIPPLE} = 99$ mVp-p

**Figure 88** – Output Voltage Ripple.  
$V_{IN} = 400$ VDC, $I_{OUT} = 0.625$ A.  
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 50 $\mu$s / div.  
$V_{RIPPLE} = 138$ mVp-p

**Figure 89** – Output Voltage Ripple.  
$V_{IN} = 550$ VDC, $I_{OUT} = 0.625$ A.  
Top Half: $V_{OUT}$, 50 mV, 5 ms / div.  
Bottom Half: Zoom @ 20 $\mu$s / div.  
$V_{RIPPLE} = 158$ mVp-p
9.3.5 0% Loading Condition

**Figure 90** – Output Voltage Ripple.
VIN = 130 VDC, IOUT = 0 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 μs / div.
VRIPPLE = 43 mVp-p

**Figure 91** – Output Voltage Ripple.
VIN = 60 VDC, IOUT = 0 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 μs / div.
VRIPPLE = 114 mVp-p

**Figure 92** – Output Voltage Ripple.
VIN = 130 VDC, IOUT = 0 A.
Top Half: VOUT, 50 mV, 5 ms / div.
Bottom Half: Zoom @ 50 μs / div.
VRIPPLE = 126 mVp-p
9.4 Output Load Transient

9.4.1 Output Load Transient, 100% to 50% Load

Figure 93 – Output Load Transient, 100% to 50% Load.
VIN = 30 VDC, IOUT = 0.85 A to 0.425 A
VOUT(MAX) = 11.79 V, VOUT(MIN) = 11.25 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 2 ms / div.

Figure 94 – Output Load Transient, 100% to 50% Load.
VIN = 60 VDC, IOUT = 1.25 A to 0.625 A.
VOUT(MAX) = 12.16 V, VOUT(MIN) = 11.53 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 2 ms / div.

Figure 95 – Output Load Transient, 100% to 50% Load.
VIN = 130 VDC, IOUT = 2.5 A to 1.25 A.
VOUT(MAX) = 12.38 V, VOUT(MIN) = 11.36 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 1 ms / div.

Figure 96 – Output Load Transient, 100% to 50% Load.
VIN = 400 VDC, IOUT = 2.5 A to 1.25 A.
VOUT(MAX) = 12.63 V, VOUT(MIN) = 11.37 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 1 ms / div.
Figure 97 – Output Load Transient, 100% to 50% Load.
$V_{IN} = 550 \text{VDC}, I_{OUT} = 2.5 \text{A to 1.25 A}$.
$V_{OUT(MAX)} = 12.74 \text{V}, V_{OUT(MIN)} = 11.34 \text{V}$.
**Upper:** $V_{OUT}$, 1 V, 100 ms / div.
**Lower:** $I_{OUT}$, 1 A, 100 ms / div.
**Bottom Half:** Zoom @ 2 ms / div.
9.4.2  Output Load Transient, 100% to 0% Load

Figure 98 – Output Load Transient, 100% to 0% Load.
VIN = 30 VDC, IOUT = 0.85 A to 0 A.
VOUT(MAX) = 12.10 V, VOUT(MIN)= 11.27 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 2 ms / div.

Figure 99 – Output Load Transient, 100% to 0% Load.
VIN = 60 VDC, IOUT = 1.25 A to 0 A.
VOUT(MAX) = 12.10 V, VOUT(MIN)= 11.49 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 2 ms / div.

Figure 100 – Output Load Transient, 100% to 0% Load.
VIN = 130 VDC, IOUT = 2.5 A to 0 A.
VOUT(MAX) = 12.36 V, VOUT(MIN)= 11.34 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 1 ms / div.

Figure 101 – Output Load Transient, 100% to 0% Load.
VIN = 400 VDC, IOUT = 2.5 A to 0 A.
VOUT(MAX) = 12.65 V, VOUT(MIN)= 11.21 V.
Upper: VOUT, 1 V, 100 ms / div.
Lower: IOUT, 1 A, 100 ms / div.
Bottom Half: Zoom @ 1 ms / div.
**Figure 102** – Output Load Transient, 100% to 0% Load.

- $V_{IN} = 550 \text{ VDC, } I_{OUT} = 2.5 \text{ A to } 1.25 \text{ A.}$
- $V_{OUT(\text{MAX})} = 12.75 \text{ V, } V_{OUT(\text{MIN})} = 11.14 \text{ V.}$
- **Upper**: $V_{OUT}$, 1 V, 100 ms / div.
- **Lower**: $I_{OUT}$, 1 A, 100 ms / div.
- Bottom Half: Zoom @ 2 ms / div.
## 9.5 Output Short-Circuit Auto-Restart Test

### Figure 103 – 30 VDC, Output Shorted.
- $V_{IN} = 30$ VDC.
- $ART_{on} = 81$ ms, $ART_{off} = 1.88$ s.
- **Upper:** $V_{OUT}$, 1 V, 1 s / div.
- **Lower:** $I_{OUT}$, 1 A, 1 s / div.
- Bottom Half: Zoom @ 10 ms / div.

### Figure 104 – 60 VDC, Output Shorted.
- $V_{IN} = 60$ VDC.
- $ART_{on} = 41$ ms, $ART_{off} = 1.55$ s.
- **Upper:** $V_{OUT}$, 1 V, 1 s / div.
- **Lower:** $I_{OUT}$, 1 A, 1 s / div.
- Bottom Half: Zoom @ 10 ms / div.

### Figure 105 – 130 VDC, Output Shorted.
- $V_{IN} = 130$ VDC.
- $ART_{on} = 50$ ms, $ART_{off} = 1.53$ s.
- **Upper:** $V_{OUT}$, 1 V, 1 s / div.
- **Lower:** $I_{OUT}$, 1 A, 1 s / div.
- Bottom Half: Zoom @ 10 ms / div.

### Figure 106 – 400 VDC, Output Shorted.
- $V_{IN} = 400$ VDC.
- $ART_{on} = 56$ ms, $ART_{off} = 1.54$ s.
- **Upper:** $V_{OUT}$, 1 V, 1 s / div.
- **Lower:** $I_{OUT}$, 1 A, 1 s / div.
- Bottom Half: Zoom @ 10 ms / div.
Figure 107 – 550 VDC, Output Shorted.

$V_{IN} = 550$ VDC.

$AR_{Ton} = 56$ ms, $AR_{Toff} = 1.54$ s.

Upper: $V_{OUT}$, 1 V, 1 s / div.
Lower: $I_{OUT}$, 1 A, 1 s / div.
Bottom Half: Zoom @ 10 ms / div.
10 Thermal Performance (SR FET)

All measurements have been done at room ambient temperature after 2 hours of continuous operation.

Figure 108 – 130 VDC 2.5 A Full Load.
Temperature of InnoSwitch3-AQ: 73.6 °C.
Temperature of SR FET: 74.3 °C.
Ambient Temperature: 28.5 °C.

Figure 109 – 400 VDC 2.5 A Full Load.
Temperature of InnoSwitch3-AQ: 69.7 °C.
Temperature of SR FET: 71.9 °C.
Ambient Temperature: 26.8 °C.

Figure 110 – 500 VDC 2.5 A Full Load.
Temperature of InnoSwitch3-AQ: 79.4 °C.
Temperature of SR FET: 75.7 °C.
Ambient Temperature: 28.2 °C.
<table>
<thead>
<tr>
<th>Component</th>
<th>130 VDC Temperature (°C)</th>
<th>400 VDC Temperature (°C)</th>
<th>500 VDC Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1 (Primary Controller) – Bx1</td>
<td>73.6</td>
<td>69.7</td>
<td>79.4</td>
</tr>
<tr>
<td>Q1, Q2 (SR FET) – Bx2</td>
<td>74.3</td>
<td>71.9</td>
<td>75.7</td>
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<tr>
<td>Ambient</td>
<td>28.5</td>
<td>26.8</td>
<td>28.2</td>
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<tr>
<td>IC temperature rise vs. ambient (delta)</td>
<td>45.1</td>
<td>42.9</td>
<td>51.2</td>
</tr>
</tbody>
</table>
10.1 **INN3977CQ Temperature Rise vs. Output Power**

![Graph showing temperature rise vs. output power for INN3977CQ](image)

**Figure 111** – Output Power vs. InnoSwitch3-AQ Temperature Rise.
### 12 Thermal Performance (Qspeed Diode)

All measurements have been done at room ambient temperature after 2 hours of continuous operation.

**Figure 112** – 130 VDC 2.5A Full Load.
- Temperature of InnoSwitch3-AQ: 73.8 ºC.
- Temperature of SR FET: 94.8 ºC.
- Ambient Temperature: 27.3 ºC.

**Figure 113** – 400 VDC 2.5A Full Load.
- Temperature of InnoSwitch3-AQ: 79.3 ºC.
- Temperature of SR FET: 100 ºC.
- Ambient Temperature: 28.3 ºC.

**Figure 114** – 500 VDC 2.5A Full Load.
- Temperature of InnoSwitch3-AQ: 84.7 ºC.
- Temperature of SR FET: 105.5 ºC.
- Ambient Temperature: 27.3 ºC.
<table>
<thead>
<tr>
<th>Component</th>
<th>130 VDC Temperature (°C)</th>
<th>400 VDC Temperature (°C)</th>
<th>500 VDC Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1 (Primary Controller) – Bx1</td>
<td>73.8</td>
<td>79.3</td>
<td>84.7</td>
</tr>
<tr>
<td>Q1 (Qspeed Diode) – Bx2</td>
<td>94.8</td>
<td>100</td>
<td>105.5</td>
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<tr>
<td>Ambient</td>
<td>27.3</td>
<td>28.3</td>
<td>27.3</td>
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<tr>
<td>IC temperature rise vs. ambient (delta)</td>
<td>46.5</td>
<td>51</td>
<td>57.4</td>
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## 13 -40 °C and +85 °C operational test

### Start-up at -40 °C full load

<table>
<thead>
<tr>
<th>Ambient (°C)</th>
<th>VIN (VDC)</th>
<th>Input Power (W)</th>
<th>Input Current (mA)</th>
<th>VOUT (V)</th>
<th>IOUT (A)</th>
<th>Efficiency (%)</th>
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</thead>
<tbody>
<tr>
<td>-40 °C</td>
<td>30</td>
<td>11.3</td>
<td>505</td>
<td>11.2</td>
<td>0.9</td>
<td>83.7</td>
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<tr>
<td></td>
<td>60</td>
<td>17.1</td>
<td>470</td>
<td>11.7</td>
<td>1.3</td>
<td>86.4</td>
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<tr>
<td></td>
<td>130</td>
<td>33.6</td>
<td>518</td>
<td>11.8</td>
<td>2.5</td>
<td>87.8</td>
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<tr>
<td></td>
<td>400</td>
<td>37.6</td>
<td>287</td>
<td>12.3</td>
<td>2.5</td>
<td>81.8</td>
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<tr>
<td></td>
<td>550</td>
<td>37.9</td>
<td>239</td>
<td>12.3</td>
<td>2.5</td>
<td>81.1</td>
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</table>

### After one hour running at full load, no OTP occurred

<table>
<thead>
<tr>
<th>Ambient (°C)</th>
<th>VIN (VDC)</th>
<th>Input Power (W)</th>
<th>Input Current (mA)</th>
<th>VOUT (V)</th>
<th>IOUT (A)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>85 °C</td>
<td>30</td>
<td>11.6</td>
<td>516</td>
<td>11.51</td>
<td>0.85</td>
<td>84.3</td>
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<td></td>
<td>60</td>
<td>16.5</td>
<td>455</td>
<td>11.66</td>
<td>1.25</td>
<td>88.3</td>
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<td>523</td>
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<td>33.5</td>
<td>298</td>
<td>11.74</td>
<td>2.5</td>
<td>87.6</td>
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<td></td>
<td>550</td>
<td>34.6</td>
<td>249</td>
<td>11.75</td>
<td>2.5</td>
<td>84.9</td>
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## 15 Revision History

<table>
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<tr>
<th>Date</th>
<th>Author</th>
<th>Revision</th>
<th>Description &amp; Changes</th>
<th>Reviewed</th>
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<tbody>
<tr>
<td>11-Feb-20</td>
<td>DK</td>
<td>1.0</td>
<td>Initial Release</td>
<td>Apps &amp; Mktg</td>
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<tr>
<td>09-Apr-20</td>
<td>KM</td>
<td>1.1</td>
<td>Added Test Point Parts</td>
<td>Apps &amp; Mktg</td>
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<td>09-Jun-20</td>
<td>KM</td>
<td>1.2</td>
<td>Converted to RDR.</td>
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<td>31-Aug-20</td>
<td>KM</td>
<td>1.3</td>
<td>Updated Figure 13.</td>
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<tr>
<td>06-Apr-21</td>
<td>DK</td>
<td>1.4</td>
<td>Updated to Rev E PCB.</td>
<td>Apps &amp; Mktg</td>
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<td>Updated BOM and Schematic.</td>
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</tbody>
</table>
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